

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRR-c encoded:
				5 *
				6 * E7F0 VAVGL - VECTOR AVERAGE LOGICAL
				7 * E7F2 VAVG - VECTOR AVERAGE
				8 * E7FC VMNL - VECTOR MINIMUM LOGICAL
				9 * E7FD VMXL - VECTOR MAXIMUM LOGICAL
				10 * E7FE VMN - VECTOR MINIMUM
				11 * E7FF VMX - VECTOR MAXIMUM
				12 *
				13 * James Wekel July 2024
				14 * July 2025 - Vector-enhancements facility 3 update
				15 *****
				17 *****
				18 *
				19 * basic instruction tests
				20 *
				21 *****
				22 * This program tests proper functioning of the z/arch E7 VRR-c vector
				23 * average, minimum and maximum instructions.
				24 * Exceptions are not tested.
				25 *
				26 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				27 * obvious coding errors. None of the tests are thorough. They are
				28 * NOT designed to test all aspects of any of the instructions.
				29 *
				30 *****
				31 *
				32 * *Testcase zvector-e7-01-MinMaxAvg: VECTOR E7 VRR-c instructions
				33 * *
				34 * * Zvector E7 instruction tests for VRR-c encoded:
				35 * *
				36 * * E7F0 VAVGL - VECTOR AVERAGE LOGICAL
				37 * * E7F2 VAVG - VECTOR AVERAGE
				38 * * E7FC VMNL - VECTOR MINIMUM LOGICAL
				39 * * E7FD VMXL - VECTOR MAXIMUM LOGICAL
				40 * * E7FE VMN - VECTOR MINIMUM
				41 * * E7FF VMX - VECTOR MAXIMUM
				42 * *
				43 * * # -----
				44 * * # This tests only the basic function of the instruction.
				45 * * # Exceptions are NOT tested.
				46 * * # -----
				47 * *
				48 * main size 2
				49 * numcpu 1
				50 * sysclear
				51 * archlvl z/Arch
				52 * *
				53 * loadcore "\$(testpath)/zvector-e7-01-MinMaxAvg.core" 0x0
				54 * *
				55 * diag8cmd enable # (needed for messages to Hercules console)
				56 * runtest 2

60	*
61	*****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				63 *****
				64 * FCHECK Macro - Is a Facility Bit set?
				65 *
				66 * If the facility bit is NOT set, an message is issued and
				67 * the test is skipped.
				68 *
				69 * Fcheck uses R0, R1 and R2
				70 *
				71 * eg. FCHECK 134, 'vector-packed-decimal'
				72 *****
				73 MACRO
				74 FCHECK &BITNO, &NOTSETMSG
				75 . * &BITNO : facility bit number to check
				76 . * &NOTSETMSG : 'facility name'
				77 LCLA &FBBYTE Facility bit in Byte
				78 LCLA &FBBIT Facility bit within Byte
				79
				80 LCLA &L(8)
				81 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				82
				83 &FBBYTE SETA &BITNO/8
				84 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				85 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				86
				87 B X&SYSNDX
				88 * Fcheck data area
				89 * skip messgae
				90 SKT&SYSNDX DC C' Skipping tests: '
				91 DC C&NOTSETMSG
				92 DC C' (bit &BITNO) is not installed.'
				93 SKL&SYSNDX EQU *-SKT&SYSNDX
				94 * facility bits
				95 DS FD gap
				96 FB&SYSNDX DS 4FD
				97 DS FD gap
				98 *
				99 X&SYSNDX EQU *
				100 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				101 STFLE FB&SYSNDX get facility bits
				102
				103 XGR R0, R0
				104 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				105 N R0, =F' &FBBIT' is bit set?
				106 BNZ XC&SYSNDX
				107 *
				108 * facility bit not set, issue message and exit
				109 *
				110 LA R0, SKL&SYSNDX message length
				111 LA R1, SKT&SYSNDX message address
				112 BAL R2, MSG
				113
				114 B EOJ
				115 XC&SYSNDX EQU *
				116 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				118	*****		
				119	* Low core PSWs		
				120	*****		
00000000		00000000	000031B7	121	ZVE7TST	START 0	
		00000000		122		USING ZVE7TST, R0	Low core addressability
		00000140	00000000	123			
				124	SVOLDPSW EQU	ZVE7TST+X' 140'	z/Arch Supervisor call old PSW
00000000		00000000	000001A0	126	ORG	ZVE7TST+X' 1A0'	z/Architecture RESTART PSW
000001A0	00000001 80000000			127	DC	X' 0000000180000000'	
000001A8	00000000 00000200			128	DC	AD(BEGIN)	
000001B0		000001B0	000001D0	130	ORG	ZVE7TST+X' 1D0'	z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			131	DC	X' 0002000180000000'	
000001D8	00000000 0000DEAD			132	DC	AD(X' DEAD')	
000001E0		000001E0	00000200	134	ORG	ZVE7TST+X' 200'	Start of actual test program..
				136	*****		
				137	* The actual "ZVE7TST" program itself...		
				138	*****		
				139	*		
				140	* Architecture Mode: z/Arch		
				141	* Register Usage:		
				142	*		
				143	R0	(work)	
				144	R1- 4	(work)	
				145	R5	Testing control table - current test base	
				146	R6- R7	(work)	
				147	R8	First base register	
				148	R9	Second base register	
				149	R10	Third base register	
				150	R11	E7TEST call return	
				151	R12	E7TESTS register	
				152	R13	(work)	
				153	R14	Subroutine call	
				154	R15	Secondary Subroutine call or work	
				155	*		
				156	*****		
00000200		00000200		158	USING	BEGIN, R8	FIRST Base Register
00000200		00001200		159	USING	BEGIN+4096, R9	SECOND Base Register
00000200		00002200		160	USING	BEGIN+8192, R10	THIRD Base Register
00000200	0580			162	BEGIN	BALR R8, 0	Inititalize FIRST base register
00000202	0680			163	BCTR	R8, 0	Inititalize FIRST base register
00000204	0680			164	BCTR	R8, 0	Inititalize FIRST base register
00000206	4190 8800		00000800	166	LA	R9, 2048(, R8)	Inititalize SECOND base register
0000020A	4190 9800		00000800	167	LA	R9, 2048(, R9)	Inititalize SECOND base register
				168			

[illegible]

[illegible]

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				375 *****
				376 * Normal completion or Abnormal termination PSWs
				377 *****
00000510	00020001 80000000			379 E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
00000520	B2B2 8310		00000510	381 E0J LPSWE E0JPSW Normal completion
00000528	00020001 80000000			383 FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
00000538	B2B2 8328		00000528	385 FAILTEST LPSWE FAILPSW Abnormal termination
				387 *****
				388 * Working Storage
				389 *****
0000053C	00000000			391 CTLR0 DS F CRO
00000540	00000000			392 DS F
00000544				394 LTORG , Literals pool
00000544	00000040			395 =F' 64'
00000548	00000002			396 =F' 2'
0000054C	000030D0			397 =A(E7TESTS)
00000550	00000001			398 =F' 1'
00000554	0000			399 =H' 0'
00000556	005F			400 =AL2(L' MSGMSG)
				401
				402 * some constants
				403
	00000400	00000001		404 K EQU 1024 One KB
	00001000	00000001		405 PAGE EQU (4*K) Size of one page
	00010000	00000001		406 K64 EQU (64*K) 64 KB
	00100000	00000001		407 MB EQU (K*K) 1 MB
				408
	AABBCCDD	00000001		409 REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		410 REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				453	*****
				454	* E7TEST DSECT
				455	*****
				457	E7TEST DSECT ,
00000000	00000000			458	TSUB DC A(0) pointer to test
00000004	0000			459	TNUM DC H' 00' Test Number
00000006	00			460	DC X' 00'
00000007	00			461	M4 DC HL1' 00' m4 used
				462	
00000008	40404040	40404040		463	OPNAME DC CL8' ' E6 name
00000010	00000000			464	V2ADDR DC A(0) address of v2 source
00000014	00000000			465	V3ADDR DC A(0) address of v3 source
00000018	00000000			466	RELEN DC A(0) RESULT LENGTH
0000001C	00000000			467	READRR DC A(0) result (expected) address
00000020	00000000	00000000		468	DS FD gap
00000028	00000000	00000000		469	V10OUTPUT DS XL16 V1 Output
00000038	00000000	00000000		470	DS FD gap
				471	
				472	* test routine will be here (from VRR-c macro)
				473	*
				474	* followed by
				475	* EXPECTED RESULT
				477	ZVE7TST CSECT ,
000010B4		00000000	000031B7	478	DS 0F
				480	*****
				481	* Macros to help build test tables
				482	*****
				484	*
				485	* macro to generate individual test
				486	*
				487	MACRO
				488	VRR_C &INST, &M4
				489	. * &INST - VRR-c instruction under test
				490	. * &m4 - m3 field
				491	
				492	GBLA &TNUM
				493	&TNUM SETA &TNUM+1
				494	
				495	DS 0FD
				496	USING *, R5 base for test data and test routine
				497	
				498	T&TNUM DC A(X&TNUM) address of test routine
				499	DC H' &TNUM test number
				500	DC X' 00'
				501	DC HL1' &M4' m4
				502	DC CL8' &INST' instruction name
				503	DC A(RE&TNUM+16) address of v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				504	DC A(RE&TNUM+32) address of v3 source
				505	DC A(16) result length
				506 REA&TNUM	DC A(RE&TNUM) result address
				507	DS FD gap
				508 V10&TNUM	DS XL16 V1 output
				509	DS FD gap
				510 . *	
				511 *	
				512 X&TNUM	DS OF
				513	LGF R1, V2ADDR load v2 source
				514	VL v22, 0(R1) use v22 to test decoder
				515	
				516	LGF R1, V3ADDR load v3 source
				517	VL v23, 0(R1) use v23 to test decoder
				518	
				519	&INST V22, V22, V23, &M4 test instruction (dest is a source)
				520	VST V22, V10&TNUM save v1 output
				521	
				522	BR R11 return
				523	
				524 RE&TNUM	DC OF xl16 expected result
				525	
				526	DROP R5
				527	MEND
				529 *	
				530 *	macro to generate table of pointers to individual tests
				531 *	
				532	MACRO
				533	PTTABLE
				534	GBLA &TNUM
				535	LCLA &CUR
				536 &CUR	SETA 1
				537 . *	
				538 TTABLE	DS OF
				539 . LOOP	ANOP
				540 . *	
				541	DC A(T&CUR) TEST &CUR
				542 . *	
				543 &CUR	SETA &CUR+1
				544	AIF (&CUR LE &TNUM) . LOOP
				545 *	
				546	DC A(0) END OF TABLE
				547	DC A(0)
				548 . *	
				549	MEND
				550	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				552 *****	
				553 * E6 VRR-c tests	
				554 *****	
				555 PRINT DATA	
				556	
				557 * E7F0 VAVGL - VECTOR AVERAGE LOGICAL	
				558 * E7F2 VAVG - VECTOR AVERAGE	
				559 * E7FC VMNL - VECTOR MINIMUM LOGICAL	
				560 * E7FD VMXL - VECTOR MAXIMUM LOGICAL	
				561 * E7FE VMN - VECTOR MINIMUM	
				562 * E7FF VMX - VECTOR MAXIMUM	
				563	
				564 * VRR-c instruction, m4	
				565 * followed by	
				566 * 16 byte expected result (V1)	
				567 * 16 byte V2 source	
				568 * 16 byte V3 source	
				569 * -----	
				570 * VMX - VECTOR MAXIMUM	
				571 * -----	
				572 * Byte	
				573 VRR_C VMX, 0	
000010B8				574+ DS OFD	
000010B8		000010B8		575+ USING *, R5	base for test data and test routine
000010B8	000010F8			576+T1 DC A(X1)	address of test routine
000010BC	0001			577+ DC H' 1'	test number
000010BE	00			578+ DC X' 00'	
000010BF	00			579+ DC HL1' 0'	m4
000010C0	E5D4E740 40404040			580+ DC CL8' VMX'	instruction name
000010C8	00001130			581+ DC A(RE1+16)	address of v2 source
000010CC	00001140			582+ DC A(RE1+32)	address of v3 source
000010D0	00000010			583+ DC A(16)	result length
000010D4	00001120			584+REA1 DC A(RE1)	result address
000010D8	00000000 00000000			585+ DS FD	gap
000010E0	00000000 00000000			586+V101 DS XL16	V1 output
000010E8	00000000 00000000				
000010F0	00000000 00000000			587+ DS FD	gap
				588+*	
000010F8				589+X1 DS 0F	
000010F8	E310 5010 0014	00000010		590+ LGF R1, V2ADDR	load v2 source
000010FE	E761 0000 0806	00000000		591+ VL v22, 0(R1)	use v22 to test decoder
00001104	E310 5014 0014	00000014		592+ LGF R1, V3ADDR	load v3 source
0000110A	E771 0000 0806	00000000		593+ VL v23, 0(R1)	use v23 to test decoder
00001110	E766 7000 0EFF			594+ VMX V22, V22, V23, 0	test instruction (dest is a source)
00001116	E760 5028 080E	000010E0		595+ VST V22, V101	save v1 output
0000111C	07FB			596+ BR R11	return
00001120				597+RE1 DC 0F	xl16 expected result
00001120				598+ DROP R5	
00001120	02030405 09010181			599 DC XL16' 0203040509010181070FFFFFE00000020'	expected result
00001128	070FFFFE 00000020				
00001130	01020304 09800181		600	DC XL16' 0102030409800181070FFFFD0000001F'	v2
00001138	070FFFFD 0000001F				
00001140	02030405 0001FF80		601	DC XL16' 020304050001FF80010AFEFE00000020'	v3
00001148	010AFEFE 00000020				
			602		
			603 * Halfword		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				604	VRR_C VMX, 1	
00001150				605+	DS OFD	
00001150		00001150		606+	USING *, R5	base for test data and test routine
00001150	00001190			607+T2	DC A(X2)	address of test routine
00001154	0002			608+	DC H' 2'	test number
00001156	00			609+	DC X' 00'	
00001157	01			610+	DC HL1' 1'	m4
00001158	E5D4E740 40404040			611+	DC CL8' VMX'	instruction name
00001160	000011C8			612+	DC A(RE2+16)	address of v2 source
00001164	000011D8			613+	DC A(RE2+32)	address of v3 source
00001168	00000010			614+	DC A(16)	result length
0000116C	000011B8			615+REA2	DC A(RE2)	result address
00001170	00000000 00000000			616+	DS FD	gap
00001178	00000000 00000000			617+V102	DS XL16	V1 output
00001180	00000000 00000000					
00001188	00000000 00000000			618+	DS FD	gap
				619+*		
00001190				620+X2	DS OF	
00001190	E310 5010 0014		00000010	621+	LGF R1, V2ADDR	load v2 source
00001196	E761 0000 0806		00000000	622+	VL v22, 0(R1)	use v22 to test decoder
0000119C	E310 5014 0014		00000014	623+	LGF R1, V3ADDR	load v3 source
000011A2	E771 0000 0806		00000000	624+	VL v23, 0(R1)	use v23 to test decoder
000011A8	E766 7000 1EFF			625+	VMX V22, V22, V23, 1	test instruction (dest is a source)
000011AE	E760 5028 080E		00001178	626+	VST V22, V102	save v1 output
000011B4	07FB			627+	BR R11	return
000011B8				628+RE2	DC OF	xl16 expected result
000011B8				629+	DROP R5	
000011B8	00020001 FFFE0001			630	DC XL16' 00020001FFFE00017FFF800112340020'	expected result
000011C0	7FFF8001 12340020					
000011C8	0001FFFF FFFD8000			631	DC XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
000011D0	7FFF8000 0123001F					
000011D8	00020001 FFFE0001			632	DC XL16' 00020001FFFE000100AA800112340020'	v3
000011E0	00AA8001 12340020					
				633		
				634 * Word		
				635	VRR_C VMX, 2	
000011E8				636+	DS OFD	
000011E8		000011E8		637+	USING *, R5	base for test data and test routine
000011E8	00001228			638+T3	DC A(X3)	address of test routine
000011EC	0003			639+	DC H' 3'	test number
000011EE	00			640+	DC X' 00'	
000011EF	02			641+	DC HL1' 2'	m4
000011F0	E5D4E740 40404040			642+	DC CL8' VMX'	instruction name
000011F8	00001260			643+	DC A(RE3+16)	address of v2 source
000011FC	00001270			644+	DC A(RE3+32)	address of v3 source
00001200	00000010			645+	DC A(16)	result length
00001204	00001250			646+REA3	DC A(RE3)	result address
00001208	00000000 00000000			647+	DS FD	gap
00001210	00000000 00000000			648+V103	DS XL16	V1 output
00001218	00000000 00000000					
00001220	00000000 00000000			649+	DS FD	gap
				650+*		
00001228				651+X3	DS OF	
00001228	E310 5010 0014		00000010	652+	LGF R1, V2ADDR	load v2 source
0000122E	E761 0000 0806		00000000	653+	VL v22, 0(R1)	use v22 to test decoder
00001234	E310 5014 0014		00000014	654+	LGF R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000123A	E771 0000 0806		00000000	655+	VL	v23, 0(R1)	use v23 to test decoder
00001240	E766 7000 2EFF			656+	VMX	V22, V22, V23, 2	test instruction (dest is a source)
00001246	E760 9010 080E		00001210	657+	VST	V22, V103	save v1 output
0000124C	07FB			658+	BR	R11	return
00001250				659+RE3	DC	0F	xl16 expected result
00001250				660+	DROP	R5	
00001250	FFFFFFFF 7FFFFFFFF			661	DC	XL16' FFFFFFFFF7FFFFFFFF1234567800000020'	expected result
00001258	12345678 00000020						
00001260	FFFFFFFF 7FFFFFFFF			662	DC	XL16' FFFFFFFFF7FFFFFFFF012345670000001F'	v2
00001268	01234567 0000001F						
00001270	FFFFFFFFE 0000000A			663	DC	XL16' FFFFFFFFFE0000000A1234567800000020'	v3
00001278	12345678 00000020						
				664			
				665 * Doubleword			
				666	VRR_C	VMX, 3	
00001280				667+	DS	0FD	
00001280		00001280		668+	USING	*, R5	base for test data and test routine
00001280	000012C0			669+T4	DC	A(X4)	address of test routine
00001284	0004			670+	DC	H' 4'	test number
00001286	00			671+	DC	X' 00'	
00001287	03			672+	DC	HL1' 3'	m4
00001288	E5D4E740 40404040			673+	DC	CL8' VMX'	instruction name
00001290	000012F8			674+	DC	A(RE4+16)	address of v2 source
00001294	00001308			675+	DC	A(RE4+32)	address of v3 source
00001298	00000010			676+	DC	A(16)	result length
0000129C	000012E8			677+REA4	DC	A(RE4)	result address
000012A0	00000000 00000000			678+	DS	FD	gap
000012A8	00000000 00000000			679+V104	DS	XL16	V1 output
000012B0	00000000 00000000						
000012B8	00000000 00000000			680+	DS	FD	gap
				681+*			
000012C0				682+X4	DS	0F	
000012C0	E310 5010 0014		00000010	683+	LGF	R1, V2ADDR	load v2 source
000012C6	E761 0000 0806		00000000	684+	VL	v22, 0(R1)	use v22 to test decoder
000012CC	E310 5014 0014		00000014	685+	LGF	R1, V3ADDR	load v3 source
000012D2	E771 0000 0806		00000000	686+	VL	v23, 0(R1)	use v23 to test decoder
000012D8	E766 7000 3EFF			687+	VMX	V22, V22, V23, 3	test instruction (dest is a source)
000012DE	E760 5028 080E		000012A8	688+	VST	V22, V104	save v1 output
000012E4	07FB			689+	BR	R11	return
000012E8				690+RE4	DC	0F	xl16 expected result
000012E8				691+	DROP	R5	
000012E8	FFFFFFFF FFFFFFFFF			692	DC	XL16' FFFFFFFFFFFFFFFFFF0000000000000020'	expected result
000012F0	00000000 00000020						
000012F8	FFFFFFFF FFFFFFFFF			693	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
00001300	00000000 0000001F						
00001308	FFFFFFFF FFFFFFFFD			694	DC	XL16' FFFFFFFFFFFFFFFFFFD000000000000020'	v3
00001310	00000000 00000020						
				695			
				696 * quadword			
				697	VRR_C	VMX, 4	
00001318				698+	DS	0FD	
00001318		00001318		699+	USING	*, R5	base for test data and test routine
00001318	00001358			700+T5	DC	A(X5)	address of test routine
0000131C	0005			701+	DC	H' 5'	test number
0000131E	00			702+	DC	X' 00'	
0000131F	04			703+	DC	HL1' 4'	m4

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001320	E5D4E740 40404040			704+	DC	CL8' VMX'	instruction name
00001328	00001390			705+	DC	A(RE5+16)	address of v2 source
0000132C	000013A0			706+	DC	A(RE5+32)	address of v3 source
00001330	00000010			707+	DC	A(16)	result length
00001334	00001380			708+REA5	DC	A(RE5)	result address
00001338	00000000 00000000			709+	DS	FD	gap
00001340	00000000 00000000			710+V105	DS	XL16	V1 output
00001348	00000000 00000000						
00001350	00000000 00000000			711+	DS	FD	gap
				712+*			
00001358				713+X5	DS	0F	
00001358	E310 5010 0014		00000010	714+	LGF	R1, V2ADDR	load v2 source
0000135E	E761 0000 0806		00000000	715+	VL	v22, 0(R1)	use v22 to test decoder
00001364	E310 5014 0014		00000014	716+	LGF	R1, V3ADDR	load v3 source
0000136A	E771 0000 0806		00000000	717+	VL	v23, 0(R1)	use v23 to test decoder
00001370	E766 7000 4EFF			718+	VMX	V22, V22, V23, 4	test instruction (dest is a source)
00001376	E760 5028 080E		00001340	719+	VST	V22, V105	save v1 output
0000137C	07FB			720+	BR	R11	return
00001380				721+RE5	DC	0F	xl16 expected result
00001380				722+	DROP	R5	
00001380	FFFFFFFF FFFFFFFF			723	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	expected result
00001388	00000000 0000001F						
00001390	FFFFFFFF FFFFFFFF			724	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
00001398	00000000 0000001F						
000013A0	FFFFFFFF FFFFFFFFD			725	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	v3
000013A8	00000000 00000020						
				726			
				727 * quadword			
				728	VRR_C	VMX, 4	
000013B0				729+	DS	0FD	
000013B0		000013B0		730+	USING	*, R5	base for test data and test routine
000013B0	000013F0			731+T6	DC	A(X6)	address of test routine
000013B4	0006			732+	DC	H' 6'	test number
000013B6	00			733+	DC	X' 00'	
000013B7	04			734+	DC	HL1' 4'	m4
000013B8	E5D4E740 40404040			735+	DC	CL8' VMX'	instruction name
000013C0	00001428			736+	DC	A(RE6+16)	address of v2 source
000013C4	00001438			737+	DC	A(RE6+32)	address of v3 source
000013C8	00000010			738+	DC	A(16)	result length
000013CC	00001418			739+REA6	DC	A(RE6)	result address
000013D0	00000000 00000000			740+	DS	FD	gap
000013D8	00000000 00000000			741+V106	DS	XL16	V1 output
000013E0	00000000 00000000						
000013E8	00000000 00000000			742+	DS	FD	gap
				743+*			
000013F0				744+X6	DS	0F	
000013F0	E310 5010 0014		00000010	745+	LGF	R1, V2ADDR	load v2 source
000013F6	E761 0000 0806		00000000	746+	VL	v22, 0(R1)	use v22 to test decoder
000013FC	E310 5014 0014		00000014	747+	LGF	R1, V3ADDR	load v3 source
00001402	E771 0000 0806		00000000	748+	VL	v23, 0(R1)	use v23 to test decoder
00001408	E766 7000 4EFF			749+	VMX	V22, V22, V23, 4	test instruction (dest is a source)
0000140E	E760 5028 080E		000013D8	750+	VST	V22, V106	save v1 output
00001414	07FB			751+	BR	R11	return
00001418				752+RE6	DC	0F	xl16 expected result
00001418				753+	DROP	R5	
00001418	0001FFFF FFFD8000			754	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001420	7FFF8000 0123001F						
00001428	0001FFFF FFFD8000			755	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
00001430	7FFF8000 0123001F						
00001438	FFFFFFFF FFFFFFFD			756	DC	XL16' FFFFFFFFFFFFFFFFD0000000000000020'	v3
00001440	00000000 00000020						
				757			
				758	* quadword		
				759	VRR_C VMX, 4		
00001448				760+	DS	0FD	
00001448		00001448		761+	USING	*, R5	base for test data and test routine
00001448	00001488			762+T7	DC	A(X7)	address of test routine
0000144C	0007			763+	DC	H' 7'	test number
0000144E	00			764+	DC	X' 00'	
0000144F	04			765+	DC	HL1' 4'	m4
00001450	E5D4E740 40404040			766+	DC	CL8' VMX'	instruction name
00001458	000014C0			767+	DC	A(RE7+16)	address of v2 source
0000145C	000014D0			768+	DC	A(RE7+32)	address of v3 source
00001460	00000010			769+	DC	A(16)	result length
00001464	000014B0			770+REA7	DC	A(RE7)	result address
00001468	00000000 00000000			771+	DS	FD	gap
00001470	00000000 00000000			772+V107	DS	XL16	V1 output
00001478	00000000 00000000						
00001480	00000000 00000000			773+	DS	FD	gap
				774+*			
00001488				775+X7	DS	0F	
00001488	E310 5010 0014		00000010	776+	LGF	R1, V2ADDR	load v2 source
0000148E	E761 0000 0806		00000000	777+	VL	v22, 0(R1)	use v22 to test decoder
00001494	E310 5014 0014		00000014	778+	LGF	R1, V3ADDR	load v3 source
0000149A	E771 0000 0806		00000000	779+	VL	v23, 0(R1)	use v23 to test decoder
000014A0	E766 7000 4EFF			780+	VMX	V22, V22, V23, 4	test instruction (dest is a source)
000014A6	E760 5028 080E		00001470	781+	VST	V22, V107	save v1 output
000014AC	07FB			782+	BR	R11	return
000014B0				783+RE7	DC	0F	xl16 expected result
000014B0				784+	DROP	R5	
000014B0	00020001 FFFE0001			785	DC	XL16' 00020001FFFE000100AA800112340020'	expected result
000014B8	00AA8001 12340020						
000014C0	0001FFFF FFFD8000			786	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
000014C8	7FFF8000 0123001F						
000014D0	00020001 FFFE0001			787	DC	XL16' 00020001FFFE000100AA800112340020'	v3
000014D8	00AA8001 12340020						
				788			
				789	* -----		
				790	* VMXL - VECTOR MAXIMUM LOGICAL		
				791	* -----		
				792	* Byte		
				793	VRR_C VMXL, 0		
000014E0				794+	DS	0FD	
000014E0		000014E0		795+	USING	*, R5	base for test data and test routine
000014E0	00001520			796+T8	DC	A(X8)	address of test routine
000014E4	0008			797+	DC	H' 8'	test number
000014E6	00			798+	DC	X' 00'	
000014E7	00			799+	DC	HL1' 0'	m4
000014E8	E5D4E7D3 40404040			800+	DC	CL8' VMXL'	instruction name
000014F0	00001558			801+	DC	A(RE8+16)	address of v2 source
000014F4	00001568			802+	DC	A(RE8+32)	address of v3 source
000014F8	00000010			803+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000014FC	00001548			804+REA8	DC	A(RE8)	result address
00001500	00000000 00000000			805+	DS	FD	gap
00001508	00000000 00000000			806+V108	DS	XL16	V1 output
00001510	00000000 00000000						
00001518	00000000 00000000			807+	DS	FD	gap
				808+*			
00001520				809+X8	DS	OF	
00001520	E310 5010 0014		00000010	810+	LGF	R1, V2ADDR	load v2 source
00001526	E761 0000 0806		00000000	811+	VL	v22, 0(R1)	use v22 to test decoder
0000152C	E310 5014 0014		00000014	812+	LGF	R1, V3ADDR	load v3 source
00001532	E771 0000 0806		00000000	813+	VL	v23, 0(R1)	use v23 to test decoder
00001538	E766 7000 0EFD			814+	VMXL	V22, V22, V23, 0	test instruction (dest is a source)
0000153E	E760 5028 080E		00001508	815+	VST	V22, V108	save v1 output
00001544	07FB			816+	BR	R11	return
00001548				817+RE8	DC	OF	xl16 expected result
00001548				818+	DROP	R5	
00001548	02030405 0980FF81			819	DC	XL16' 020304050980FF81070FFFFFE00000020'	expected result
00001550	070FFFFE 00000020						
00001558	01020304 09800181			820	DC	XL16' 0102030409800181070FFFFD0000001F'	v2
00001560	070FFFFD 0000001F						
00001568	02030405 0001FF80			821	DC	XL16' 020304050001FF80010AFEFE00000020'	v3
00001570	010AFEFE 00000020						
				822			
				823 * Halfword			
				824	VRR_C	VMXL, 1	
00001578				825+	DS	OFD	
00001578		00001578		826+	USING	*, R5	base for test data and test routine
00001578	000015B8			827+T9	DC	A(X9)	address of test routine
0000157C	0009			828+	DC	H' 9'	test number
0000157E	00			829+	DC	X' 00'	
0000157F	01			830+	DC	HL1' 1'	m4
00001580	E5D4E7D3 40404040			831+	DC	CL8' VMXL'	instruction name
00001588	000015F0			832+	DC	A(RE9+16)	address of v2 source
0000158C	00001600			833+	DC	A(RE9+32)	address of v3 source
00001590	00000010			834+	DC	A(16)	result length
00001594	000015E0			835+REA9	DC	A(RE9)	result address
00001598	00000000 00000000			836+	DS	FD	gap
000015A0	00000000 00000000			837+V109	DS	XL16	V1 output
000015A8	00000000 00000000						
000015B0	00000000 00000000			838+	DS	FD	gap
				839+*			
000015B8				840+X9	DS	OF	
000015B8	E310 5010 0014		00000010	841+	LGF	R1, V2ADDR	load v2 source
000015BE	E761 0000 0806		00000000	842+	VL	v22, 0(R1)	use v22 to test decoder
000015C4	E310 5014 0014		00000014	843+	LGF	R1, V3ADDR	load v3 source
000015CA	E771 0000 0806		00000000	844+	VL	v23, 0(R1)	use v23 to test decoder
000015D0	E766 7000 1EFD			845+	VMXL	V22, V22, V23, 1	test instruction (dest is a source)
000015D6	E760 5028 080E		000015A0	846+	VST	V22, V109	save v1 output
000015DC	07FB			847+	BR	R11	return
000015E0				848+RE9	DC	OF	xl16 expected result
000015E0				849+	DROP	R5	
000015E0	0002FFFF FFFE8000			850	DC	XL16' 0002FFFFF80007FFF800112340020'	expected result
000015E8	7FFF8001 12340020						
000015F0	0001FFFF FFFD8000			851	DC	XL16' 0001FFFFF80007FFF80000123001F'	v2
000015F8	7FFF8000 0123001F						
00001600	00020001 FFFE0001			852	DC	XL16' 00020001FFFE000100AA800112340020'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001608	00AA8001 12340020			853		
				854 * Word		
				855	VRR_C VMKL, 2	
00001610				856+	DS OFD	
00001610		00001610		857+	USING *, R5	base for test data and test routine
00001610	00001650			858+T10	DC A(X10)	address of test routine
00001614	000A			859+	DC H' 10'	test number
00001616	00			860+	DC X' 00'	
00001617	02			861+	DC HL1' 2'	m4
00001618	E5D4E7D3 40404040			862+	DC CL8' VMKL'	instruction name
00001620	00001688			863+	DC A(RE10+16)	address of v2 source
00001624	00001698			864+	DC A(RE10+32)	address of v3 source
00001628	00000010			865+	DC A(16)	result length
0000162C	00001678			866+REA10	DC A(RE10)	result address
00001630	00000000 00000000			867+	DS FD	gap
00001638	00000000 00000000			868+V1010	DS XL16	V1 output
00001640	00000000 00000000					
00001648	00000000 00000000			869+	DS FD	gap
				870+*		
00001650				871+X10	DS OF	
00001650	E310 5010 0014		00000010	872+	LGF R1, V2ADDR	load v2 source
00001656	E761 0000 0806		00000000	873+	VL v22, 0(R1)	use v22 to test decoder
0000165C	E310 5014 0014		00000014	874+	LGF R1, V3ADDR	load v3 source
00001662	E771 0000 0806		00000000	875+	VL v23, 0(R1)	use v23 to test decoder
00001668	E766 7000 2EFD			876+	VMKL V22, V22, V23, 2	test instruction (dest is a source)
0000166E	E760 5028 080E		00001638	877+	VST V22, V1010	save v1 output
00001674	07FB			878+	BR R11	return
00001678				879+RE10	DC OF	xl16 expected result
00001678				880+	DROP R5	
00001678	FFFFFFFF 7FFFFFFFFF			881	DC XL16' FFFFFFFFFF7FFFFFFFFF1234567800000020'	expected result
00001680	12345678 00000020					
00001688	FFFFFFFF 7FFFFFFFFF			882	DC XL16' FFFFFFFFFF7FFFFFFFFF012345670000001F'	v2
00001690	01234567 0000001F					
00001698	FFFFFFFFE 0000000A			883	DC XL16' FFFFFFFFE0000000A1234567800000020'	v3
000016A0	12345678 00000020					
				884		
				885 * Doubleword		
				886	VRR_C VMKL, 3	
000016A8				887+	DS OFD	
000016A8		000016A8		888+	USING *, R5	base for test data and test routine
000016A8	000016E8			889+T11	DC A(X11)	address of test routine
000016AC	000B			890+	DC H' 11'	test number
000016AE	00			891+	DC X' 00'	
000016AF	03			892+	DC HL1' 3'	m4
000016B0	E5D4E7D3 40404040			893+	DC CL8' VMKL'	instruction name
000016B8	00001720			894+	DC A(RE11+16)	address of v2 source
000016BC	00001730			895+	DC A(RE11+32)	address of v3 source
000016C0	00000010			896+	DC A(16)	result length
000016C4	00001710			897+REA11	DC A(RE11)	result address
000016C8	00000000 00000000			898+	DS FD	gap
000016D0	00000000 00000000			899+V1011	DS XL16	V1 output
000016D8	00000000 00000000					
000016E0	00000000 00000000			900+	DS FD	gap
				901+*		
000016E8				902+X11	DS OF	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000016E8	E310 5010 0014		00000010	903+	LGF	R1, V2ADDR	load v2 source
000016EE	E761 0000 0806		00000000	904+	VL	v22, 0(R1)	use v22 to test decoder
000016F4	E310 5014 0014		00000014	905+	LGF	R1, V3ADDR	load v3 source
000016FA	E771 0000 0806		00000000	906+	VL	v23, 0(R1)	use v23 to test decoder
00001700	E766 7000 3EFD			907+	VMXL	V22, V22, V23, 3	test instruction (dest is a source)
00001706	E760 5028 080E		000016D0	908+	VST	V22, V1011	save v1 output
0000170C	07FB			909+	BR	R11	return
00001710				910+RE11	DC	0F	xl16 expected result
00001710				911+	DROP	R5	
00001710	FFFFFFFF FFFFFFFF			912	DC	XL16' FFFFFFFFFFFFFFFFFF0000000000000020'	expected result
00001718	00000000 00000020						
00001720	FFFFFFFF FFFFFFFF			913	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
00001728	00000000 0000001F						
00001730	FFFFFFFF FFFFFFFFD			914	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	v3
00001738	00000000 00000020						
				915			
				916 * quadword			
				917	VRR_C	VMXL, 4	
00001740				918+	DS	0FD	
00001740		00001740		919+	USING	*, R5	base for test data and test routine
00001740	00001780			920+T12	DC	A(X12)	address of test routine
00001744	000C			921+	DC	H' 12'	test number
00001746	00			922+	DC	X' 00'	
00001747	04			923+	DC	HL1' 4'	m4
00001748	E5D4E7D3 40404040			924+	DC	CL8' VMXL'	instruction name
00001750	000017B8			925+	DC	A(RE12+16)	address of v2 source
00001754	000017C8			926+	DC	A(RE12+32)	address of v3 source
00001758	00000010			927+	DC	A(16)	result length
0000175C	000017A8			928+REA12	DC	A(RE12)	result address
00001760	00000000 00000000			929+	DS	FD	gap
00001768	00000000 00000000			930+V1012	DS	XL16	V1 output
00001770	00000000 00000000						
00001778	00000000 00000000			931+	DS	FD	gap
				932+*			
00001780				933+X12	DS	0F	
00001780	E310 5010 0014		00000010	934+	LGF	R1, V2ADDR	load v2 source
00001786	E761 0000 0806		00000000	935+	VL	v22, 0(R1)	use v22 to test decoder
0000178C	E310 5014 0014		00000014	936+	LGF	R1, V3ADDR	load v3 source
00001792	E771 0000 0806		00000000	937+	VL	v23, 0(R1)	use v23 to test decoder
00001798	E766 7000 4EFD			938+	VMXL	V22, V22, V23, 4	test instruction (dest is a source)
0000179E	E760 5028 080E		00001768	939+	VST	V22, V1012	save v1 output
000017A4	07FB			940+	BR	R11	return
000017A8				941+RE12	DC	0F	xl16 expected result
000017A8				942+	DROP	R5	
000017A8	FFFFFFFF FFFFFFFF			943	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	expected result
000017B0	00000000 0000001F						
000017B8	FFFFFFFF FFFFFFFF			944	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
000017C0	00000000 0000001F						
000017C8	FFFFFFFF FFFFFFFFD			945	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	v3
000017D0	00000000 00000020						
				946			
				947 * quadword			
				948	VRR_C	VMXL, 4	
000017D8				949+	DS	0FD	
000017D8		000017D8		950+	USING	*, R5	base for test data and test routine
000017D8	00001818			951+T13	DC	A(X13)	address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000017DC	000D			952+	DC	H' 13' test number
000017DE	00			953+	DC	X' 00'
000017DF	04			954+	DC	HL1' 4' m4
000017E0	E5D4E7D3 40404040			955+	DC	CL8' VMXL' instruction name
000017E8	00001850			956+	DC	A(RE13+16) address of v2 source
000017EC	00001860			957+	DC	A(RE13+32) address of v3 source
000017F0	00000010			958+	DC	A(16) result length
000017F4	00001840			959+REA13	DC	A(RE13) result address
000017F8	00000000 00000000			960+	DS	FD gap
00001800	00000000 00000000			961+V1013	DS	XL16 V1 output
00001808	00000000 00000000					
00001810	00000000 00000000			962+	DS	FD gap
				963+*		
00001818				964+X13	DS	0F
00001818	E310 5010 0014		00000010	965+	LGF	R1, V2ADDR load v2 source
0000181E	E761 0000 0806		00000000	966+	VL	v22, 0(R1) use v22 to test decoder
00001824	E310 5014 0014		00000014	967+	LGF	R1, V3ADDR load v3 source
0000182A	E771 0000 0806		00000000	968+	VL	v23, 0(R1) use v23 to test decoder
00001830	E766 7000 4EFD			969+	VMXL	V22, V22, V23, 4 test instruction (dest is a source)
00001836	E760 5028 080E		00001800	970+	VST	V22, V1013 save v1 output
0000183C	07FB			971+	BR	R11 return
00001840				972+RE13	DC	0F xl16 expected result
00001840				973+	DROP	R5
00001840	FFFFFFFF FFFFFFFD			974	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020' expected result
00001848	00000000 00000020					
00001850	0001FFFF FFFD8000			975	DC	XL16' 0001FFFF FFFD80007FFF80000123001F' v2
00001858	7FFF8000 0123001F					
00001860	FFFFFFFF FFFFFFFD			976	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020' v3
00001868	00000000 00000020					
				977		
				978 * quadword		
				979	VRR_C	VMXL, 4
00001870				980+	DS	0FD
00001870		00001870		981+	USING	*, R5 base for test data and test routine
00001870	000018B0			982+T14	DC	A(X14) address of test routine
00001874	000E			983+	DC	H' 14' test number
00001876	00			984+	DC	X' 00'
00001877	04			985+	DC	HL1' 4' m4
00001878	E5D4E7D3 40404040			986+	DC	CL8' VMXL' instruction name
00001880	000018E8			987+	DC	A(RE14+16) address of v2 source
00001884	000018F8			988+	DC	A(RE14+32) address of v3 source
00001888	00000010			989+	DC	A(16) result length
0000188C	000018D8			990+REA14	DC	A(RE14) result address
00001890	00000000 00000000			991+	DS	FD gap
00001898	00000000 00000000			992+V1014	DS	XL16 V1 output
000018A0	00000000 00000000					
000018A8	00000000 00000000			993+	DS	FD gap
				994+*		
000018B0				995+X14	DS	0F
000018B0	E310 5010 0014		00000010	996+	LGF	R1, V2ADDR load v2 source
000018B6	E761 0000 0806		00000000	997+	VL	v22, 0(R1) use v22 to test decoder
000018BC	E310 5014 0014		00000014	998+	LGF	R1, V3ADDR load v3 source
000018C2	E771 0000 0806		00000000	999+	VL	v23, 0(R1) use v23 to test decoder
000018C8	E766 7000 4EFD			1000+	VMXL	V22, V22, V23, 4 test instruction (dest is a source)
000018CE	E760 5028 080E		00001898	1001+	VST	V22, V1014 save v1 output
000018D4	07FB			1002+	BR	R11 return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000018D8				1003+RE14	DC	0F	xl16 expected result
000018D8				1004+	DROP	R5	
000018D8	00020001 FFFE0001			1005	DC	XL16' 00020001FFFE000100AA800112340020'	expected result
000018E0	00AA8001 12340020						
000018E8	0001FFFF FFFD8000			1006	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
000018F0	7FFF8000 0123001F						
000018F8	00020001 FFFE0001			1007	DC	XL16' 00020001FFFE000100AA800112340020'	v3
00001900	00AA8001 12340020						
				1008			
				1009 *			
				1010 * VMN		- VECTOR MINIMUM	
				1011 *			
				1012 * Byte			
				1013	VRR_C	VMN, 0	
00001908				1014+	DS	0FD	
00001908		00001908		1015+	USING	*, R5	base for test data and test routine
00001908	00001948			1016+T15	DC	A(X15)	address of test routine
0000190C	000F			1017+	DC	H' 15'	test number
0000190E	00			1018+	DC	X' 00'	
0000190F	00			1019+	DC	HL1' 0'	m4
00001910	E5D4D540 40404040			1020+	DC	CL8' VMN'	instruction name
00001918	00001980			1021+	DC	A(RE15+16)	address of v2 source
0000191C	00001990			1022+	DC	A(RE15+32)	address of v3 source
00001920	00000010			1023+	DC	A(16)	result length
00001924	00001970			1024+REA15	DC	A(RE15)	result address
00001928	00000000 00000000			1025+	DS	FD	gap
00001930	00000000 00000000			1026+V1015	DS	XL16	V1 output
00001938	00000000 00000000						
00001940	00000000 00000000			1027+	DS	FD	gap
				1028+*			
00001948				1029+X15	DS	0F	
00001948	E310 5010 0014		00000010	1030+	LGF	R1, V2ADDR	load v2 source
0000194E	E761 0000 0806		00000000	1031+	VL	v22, 0(R1)	use v22 to test decoder
00001954	E310 5014 0014		00000014	1032+	LGF	R1, V3ADDR	load v3 source
0000195A	E771 0000 0806		00000000	1033+	VL	v23, 0(R1)	use v23 to test decoder
00001960	E766 7000 0EFE			1034+	VMN	V22, V22, V23, 0	test instruction (dest is a source)
00001966	E760 5028 080E		00001930	1035+	VST	V22, V1015	save v1 output
0000196C	07FB			1036+	BR	R11	return
00001970				1037+RE15	DC	0F	xl16 expected result
00001970				1038+	DROP	R5	
00001970	01020304 0080FF80			1039	DC	XL16' 010203040080FF80010AFEFD0000001F'	expected result
00001978	010AFEFD 0000001F						
00001980	01020304 09800181			1040	DC	XL16' 0102030409800181070FFFFD0000001F'	v2
00001988	070FFFFD 0000001F						
00001990	02030405 0001FF80			1041	DC	XL16' 020304050001FF80010AFEFE00000020'	v3
00001998	010AFEFE 00000020						
				1042			
				1043 * Hal fword			
				1044	VRR_C	VMN, 1	
000019A0				1045+	DS	0FD	
000019A0		000019A0		1046+	USING	*, R5	base for test data and test routine
000019A0	000019E0			1047+T16	DC	A(X16)	address of test routine
000019A4	0010			1048+	DC	H' 16'	test number
000019A6	00			1049+	DC	X' 00'	
000019A7	01			1050+	DC	HL1' 1'	m4
000019A8	E5D4D540 40404040			1051+	DC	CL8' VMN'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000019B0	00001A18			1052+	DC	A(RE16+16)	address of v2 source
000019B4	00001A28			1053+	DC	A(RE16+32)	address of v3 source
000019B8	00000010			1054+	DC	A(16)	result length
000019BC	00001A08			1055+REA16	DC	A(RE16)	result address
000019C0	00000000 00000000			1056+	DS	FD	gap
000019C8	00000000 00000000			1057+V1016	DS	XL16	V1 output
000019D0	00000000 00000000						
000019D8	00000000 00000000			1058+	DS	FD	gap
				1059+*			
000019E0				1060+X16	DS	0F	
000019E0	E310 5010 0014		00000010	1061+	LGF	R1, V2ADDR	load v2 source
000019E6	E761 0000 0806		00000000	1062+	VL	v22, 0(R1)	use v22 to test decoder
000019EC	E310 5014 0014		00000014	1063+	LGF	R1, V3ADDR	load v3 source
000019F2	E771 0000 0806		00000000	1064+	VL	v23, 0(R1)	use v23 to test decoder
000019F8	E766 7000 1EFE			1065+	VMN	V22, V22, V23, 1	test instruction (dest is a source)
000019FE	E760 5028 080E		000019C8	1066+	VST	V22, V1016	save v1 output
00001A04	07FB			1067+	BR	R11	return
00001A08				1068+RE16	DC	0F	xl16 expected result
00001A08				1069+	DROP	R5	
00001A08	0001FFFF FFFD8000			1070	DC	XL16' 0001FFFFFFFFFD800000AA80000123001F'	expected result
00001A10	00AA8000 0123001F						
00001A18	0001FFFF FFFD8000			1071	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
00001A20	7FFF8000 0123001F						
00001A28	00020001 FFFE0001			1072	DC	XL16' 00020001FFFE000100AA800112340020'	v3
00001A30	00AA8001 12340020						
				1073			
				1074 * Word			
				1075	VRR_C	VMN, 2	
00001A38				1076+	DS	0FD	
00001A38		00001A38		1077+	USING	*, R5	base for test data and test routine
00001A38	00001A78			1078+T17	DC	A(X17)	address of test routine
00001A3C	0011			1079+	DC	H' 17'	test number
00001A3E	00			1080+	DC	X' 00'	
00001A3F	02			1081+	DC	HL1' 2'	m4
00001A40	E5D4D540 40404040			1082+	DC	CL8' VMN'	instruction name
00001A48	00001AB0			1083+	DC	A(RE17+16)	address of v2 source
00001A4C	00001AC0			1084+	DC	A(RE17+32)	address of v3 source
00001A50	00000010			1085+	DC	A(16)	result length
00001A54	00001AA0			1086+REA17	DC	A(RE17)	result address
00001A58	00000000 00000000			1087+	DS	FD	gap
00001A60	00000000 00000000			1088+V1017	DS	XL16	V1 output
00001A68	00000000 00000000						
00001A70	00000000 00000000			1089+	DS	FD	gap
				1090+*			
00001A78				1091+X17	DS	0F	
00001A78	E310 5010 0014		00000010	1092+	LGF	R1, V2ADDR	load v2 source
00001A7E	E761 0000 0806		00000000	1093+	VL	v22, 0(R1)	use v22 to test decoder
00001A84	E310 5014 0014		00000014	1094+	LGF	R1, V3ADDR	load v3 source
00001A8A	E771 0000 0806		00000000	1095+	VL	v23, 0(R1)	use v23 to test decoder
00001A90	E766 7000 2EFE			1096+	VMN	V22, V22, V23, 2	test instruction (dest is a source)
00001A96	E760 5028 080E		00001A60	1097+	VST	V22, V1017	save v1 output
00001A9C	07FB			1098+	BR	R11	return
00001AA0				1099+RE17	DC	0F	xl16 expected result
00001AA0				1100+	DROP	R5	
00001AA0	FFFFFFFFE 0000000A			1101	DC	XL16' FFFFFFFFFE0000000A012345670000001F'	expected result
00001AA8	01234567 0000001F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001AB0	FFFFFFFF 7FFFFFFF			1102	DC	XL16' FFFFFFFF7FFFFFFF012345670000001F'	v2
00001AB8	01234567 0000001F						
00001AC0	FFFFFFFE 0000000A			1103	DC	XL16' FFFFFFFE0000000A1234567800000020'	v3
00001AC8	12345678 00000020						
				1104			
				1105	* Doubleword		
				1106	VRR_C	VMN, 3	
00001AD0				1107+	DS	OFD	
00001AD0		00001AD0		1108+	USING	*, R5	base for test data and test routine
00001AD0	00001B10			1109+T18	DC	A(X18)	address of test routine
00001AD4	0012			1110+	DC	H' 18'	test number
00001AD6	00			1111+	DC	X' 00'	
00001AD7	03			1112+	DC	HL1' 3'	m4
00001AD8	E5D4D540 40404040			1113+	DC	CL8' VMN'	instruction name
00001AE0	00001B48			1114+	DC	A(RE18+16)	address of v2 source
00001AE4	00001B58			1115+	DC	A(RE18+32)	address of v3 source
00001AE8	00000010			1116+	DC	A(16)	result length
00001AEC	00001B38			1117+REA18	DC	A(RE18)	result address
00001AF0	00000000 00000000			1118+	DS	FD	gap
00001AF8	00000000 00000000			1119+V1018	DS	XL16	V1 output
00001B00	00000000 00000000						
00001B08	00000000 00000000			1120+	DS	FD	gap
				1121+*			
00001B10				1122+X18	DS	OF	
00001B10	E310 5010 0014		00000010	1123+	LGF	R1, V2ADDR	load v2 source
00001B16	E761 0000 0806		00000000	1124+	VL	v22, 0(R1)	use v22 to test decoder
00001B1C	E310 5014 0014		00000014	1125+	LGF	R1, V3ADDR	load v3 source
00001B22	E771 0000 0806		00000000	1126+	VL	v23, 0(R1)	use v23 to test decoder
00001B28	E766 7000 3EFE			1127+	VMN	V22, V22, V23, 3	test instruction (dest is a source)
00001B2E	E760 5028 080E		00001AF8	1128+	VST	V22, V1018	save v1 output
00001B34	07FB			1129+	BR	R11	return
00001B38				1130+RE18	DC	OF	xl16 expected result
00001B38				1131+	DROP	R5	
00001B38	FFFFFFFF FFFFFFFD			1132	DC	XL16' FFFFFFFF000000000000001F'	expected result
00001B40	00000000 0000001F						
00001B48	FFFFFFFF FFFFFFFF			1133	DC	XL16' FFFFFFFF000000000000001F'	v2
00001B50	00000000 0000001F						
00001B58	FFFFFFFF FFFFFFFD			1134	DC	XL16' FFFFFFFF0000000000000020'	v3
00001B60	00000000 00000020						
				1135			
				1136			
				1137	* quadword		
				1138	VRR_C	VMN, 4	
00001B68				1139+	DS	OFD	
00001B68		00001B68		1140+	USING	*, R5	base for test data and test routine
00001B68	00001BA8			1141+T19	DC	A(X19)	address of test routine
00001B6C	0013			1142+	DC	H' 19'	test number
00001B6E	00			1143+	DC	X' 00'	
00001B6F	04			1144+	DC	HL1' 4'	m4
00001B70	E5D4D540 40404040			1145+	DC	CL8' VMN'	instruction name
00001B78	00001BE0			1146+	DC	A(RE19+16)	address of v2 source
00001B7C	00001BF0			1147+	DC	A(RE19+32)	address of v3 source
00001B80	00000010			1148+	DC	A(16)	result length
00001B84	00001BD0			1149+REA19	DC	A(RE19)	result address
00001B88	00000000 00000000			1150+	DS	FD	gap
00001B90	00000000 00000000			1151+V1019	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001B98	00000000 00000000						
00001BA0	00000000 00000000			1152+	DS	FD	gap
				1153+*			
00001BA8				1154+X19	DS	0F	
00001BA8	E310 5010 0014		00000010	1155+	LGF	R1, V2ADDR	load v2 source
00001BAE	E761 0000 0806		00000000	1156+	VL	v22, 0(R1)	use v22 to test decoder
00001BB4	E310 5014 0014		00000014	1157+	LGF	R1, V3ADDR	load v3 source
00001BBA	E771 0000 0806		00000000	1158+	VL	v23, 0(R1)	use v23 to test decoder
00001BC0	E766 7000 4EFE			1159+	VMN	V22, V22, V23, 4	test instruction (dest is a source)
00001BC6	E760 5028 080E		00001B90	1160+	VST	V22, V1019	save v1 output
00001BCC	07FB			1161+	BR	R11	return
00001BD0				1162+RE19	DC	0F	xl16 expected result
00001BD0				1163+	DROP	R5	
00001BD0	FFFFFFFF FFFFFFFD			1164	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020'	expected result
00001BD8	00000000 00000020						
00001BE0	FFFFFFFF FFFFFFFF			1165	DC	XL16' FFFFFFFF FFFFFFFF000000000000001F'	v2
00001BE8	00000000 0000001F						
00001BF0	FFFFFFFF FFFFFFFD			1166	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020'	v3
00001BF8	00000000 00000020						
				1167			
				1168 * quadword			
				1169	VRR_C	VMN, 4	
00001C00				1170+	DS	0FD	
00001C00		00001C00		1171+	USING	*, R5	base for test data and test routine
00001C00	00001C40			1172+T20	DC	A(X20)	address of test routine
00001C04	0014			1173+	DC	H' 20'	test number
00001C06	00			1174+	DC	X' 00'	
00001C07	04			1175+	DC	HL1' 4'	m4
00001C08	E5D4D540 40404040			1176+	DC	CL8' VMN'	instruction name
00001C10	00001C78			1177+	DC	A(RE20+16)	address of v2 source
00001C14	00001C88			1178+	DC	A(RE20+32)	address of v3 source
00001C18	00000010			1179+	DC	A(16)	result length
00001C1C	00001C68			1180+REA20	DC	A(RE20)	result address
00001C20	00000000 00000000			1181+	DS	FD	gap
00001C28	00000000 00000000			1182+V1020	DS	XL16	V1 output
00001C30	00000000 00000000						
00001C38	00000000 00000000			1183+	DS	FD	gap
				1184+*			
00001C40				1185+X20	DS	0F	
00001C40	E310 5010 0014		00000010	1186+	LGF	R1, V2ADDR	load v2 source
00001C46	E761 0000 0806		00000000	1187+	VL	v22, 0(R1)	use v22 to test decoder
00001C4C	E310 5014 0014		00000014	1188+	LGF	R1, V3ADDR	load v3 source
00001C52	E771 0000 0806		00000000	1189+	VL	v23, 0(R1)	use v23 to test decoder
00001C58	E766 7000 4EFE			1190+	VMN	V22, V22, V23, 4	test instruction (dest is a source)
00001C5E	E760 5028 080E		00001C28	1191+	VST	V22, V1020	save v1 output
00001C64	07FB			1192+	BR	R11	return
00001C68				1193+RE20	DC	0F	xl16 expected result
00001C68				1194+	DROP	R5	
00001C68	FFFFFFFF FFFFFFFD			1195	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020'	expected result
00001C70	00000000 00000020						
00001C78	0001FFFF FFFD8000			1196	DC	XL16' 0001FFFF FFFD80007FFF80000123001F'	v2
00001C80	7FFF8000 0123001F						
00001C88	FFFFFFFF FFFFFFFD			1197	DC	XL16' FFFFFFFF FFFFFFFD0000000000000020'	v3
00001C90	00000000 00000020						
				1198			
				1199 * quadword			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C98				1200	VRR_C VMN, 4		
00001C98				1201+	DS OFD		
00001C98		00001C98		1202+	USING *, R5	base for test data and test routine	
00001C98	00001CD8			1203+T21	DC A(X21)	address of test routine	
00001C9C	0015			1204+	DC H' 21'	test number	
00001C9E	00			1205+	DC X' 00'		
00001C9F	04			1206+	DC HL1' 4'	m4	
00001CA0	E5D4D540 40404040			1207+	DC CL8' VMN'	instruction name	
00001CA8	00001D10			1208+	DC A(RE21+16)	address of v2 source	
00001CAC	00001D20			1209+	DC A(RE21+32)	address of v3 source	
00001CB0	00000010			1210+	DC A(16)	result length	
00001CB4	00001D00			1211+REA21	DC A(RE21)	result address	
00001CB8	00000000 00000000			1212+	DS FD	gap	
00001CC0	00000000 00000000			1213+V1021	DS XL16	V1 output	
00001CC8	00000000 00000000						
00001CD0	00000000 00000000			1214+	DS FD	gap	
				1215+*			
00001CD8				1216+X21	DS OF		
00001CD8	E310 5010 0014		00000010	1217+	LGF R1, V2ADDR	load v2 source	
00001CDE	E761 0000 0806		00000000	1218+	VL v22, 0(R1)	use v22 to test decoder	
00001CE4	E310 5014 0014		00000014	1219+	LGF R1, V3ADDR	load v3 source	
00001CEA	E771 0000 0806		00000000	1220+	VL v23, 0(R1)	use v23 to test decoder	
00001CF0	E766 7000 4EFE			1221+	VMN V22, V22, V23, 4	test instruction (dest is a source)	
00001CF6	E760 5028 080E		00001CC0	1222+	VST V22, V1021	save v1 output	
00001CFC	07FB			1223+	BR R11	return	
00001D00				1224+RE21	DC OF	xl16 expected result	
00001D00				1225+	DROP R5		
00001D00	0001FFFF FFFD8000			1226	DC XL16' 0001FFFFFFFFFD80007FFF80000123001F'	expected result	
00001D08	7FFF8000 0123001F						
00001D10	0001FFFF FFFD8000			1227	DC XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2	
00001D18	7FFF8000 0123001F						
00001D20	00020001 FFFE0001			1228	DC XL16' 00020001FFFE000100AA800112340020'	v3	
00001D28	00AA8001 12340020						
				1229			
				1230 *	-----		
				1231 * VMNL	- VECTOR MINIMUM LOGICAL		
				1232 *	-----		
				1233 * Byte			
				1234	VRR_C VMNL, 0		
00001D30				1235+	DS OFD		
00001D30		00001D30		1236+	USING *, R5	base for test data and test routine	
00001D30	00001D70			1237+T22	DC A(X22)	address of test routine	
00001D34	0016			1238+	DC H' 22'	test number	
00001D36	00			1239+	DC X' 00'		
00001D37	00			1240+	DC HL1' 0'	m4	
00001D38	E5D4D5D3 40404040			1241+	DC CL8' VMNL'	instruction name	
00001D40	00001DA8			1242+	DC A(RE22+16)	address of v2 source	
00001D44	00001DB8			1243+	DC A(RE22+32)	address of v3 source	
00001D48	00000010			1244+	DC A(16)	result length	
00001D4C	00001D98			1245+REA22	DC A(RE22)	result address	
00001D50	00000000 00000000			1246+	DS FD	gap	
00001D58	00000000 00000000			1247+V1022	DS XL16	V1 output	
00001D60	00000000 00000000						
00001D68	00000000 00000000			1248+	DS FD	gap	
				1249+*			
00001D70				1250+X22	DS OF		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00001D70	E310 5010 0014		00000010	1251+	LGF	R1, V2ADDR	load v2 source	
00001D76	E761 0000 0806		00000000	1252+	VL	v22, 0(R1)	use v22 to test decoder	
00001D7C	E310 5014 0014		00000014	1253+	LGF	R1, V3ADDR	load v3 source	
00001D82	E771 0000 0806		00000000	1254+	VL	v23, 0(R1)	use v23 to test decoder	
00001D88	E766 7000 0EFC			1255+	VMNL	V22, V22, V23, 0	test instruction (dest is a source)	
00001D8E	E760 5028 080E		00001D58	1256+	VST	V22, V1022	save v1 output	
00001D94	07FB			1257+	BR	R11	return	
00001D98				1258+RE22	DC	0F	xl16 expected result	
00001D98				1259+	DROP	R5		
00001D98	01020304 00010180			1260	DC	XL16' 0102030400010180010AFEFD0000001F'	expected result	
00001DA0	010AFEFD 0000001F							
00001DA8	01020304 09800181			1261	DC	XL16' 0102030409800181070FFFFD0000001F'	v2	
00001DB0	070FFFFD 0000001F							
00001DB8	02030405 0001FF80			1262	DC	XL16' 020304050001FF80010AFEFE00000020'	v3	
00001DC0	010AFEFE 00000020							
				1263				
				1264 * Hal fword				
00001DC8				1265	VRR_C	VMNL, 1		
00001DC8		00001DC8		1266+	DS	0FD		
00001DC8	00001E08			1267+	USING	*, R5	base for test data and test routine	
00001DCC	0017			1268+T23	DC	A(X23)	address of test routine	
00001DCE	00			1269+	DC	H' 23'	test number	
00001DCF	01			1270+	DC	X' 00'		
00001DD0	E5D4D5D3 40404040			1271+	DC	HL1' 1'	m4	
00001DD8	00001E40			1272+	DC	CL8' VMNL'	instruction name	
00001DDC	00001E50			1273+	DC	A(RE23+16)	address of v2 source	
00001DE0	00000010			1274+	DC	A(RE23+32)	address of v3 source	
00001DE4	00001E30			1275+	DC	A(16)	result length	
00001DE8	00000000 00000000			1276+REA23	DC	A(RE23)	result address	
00001DF0	00000000 00000000			1277+	DS	FD	gap	
00001DF8	00000000 00000000			1278+V1023	DS	XL16	V1 output	
00001E00	00000000 00000000			1279+	DS	FD	gap	
				1280+*				
00001E08				1281+X23	DS	0F		
00001E08	E310 5010 0014		00000010	1282+	LGF	R1, V2ADDR	load v2 source	
00001E0E	E761 0000 0806		00000000	1283+	VL	v22, 0(R1)	use v22 to test decoder	
00001E14	E310 5014 0014		00000014	1284+	LGF	R1, V3ADDR	load v3 source	
00001E1A	E771 0000 0806		00000000	1285+	VL	v23, 0(R1)	use v23 to test decoder	
00001E20	E766 7000 1EFC			1286+	VMNL	V22, V22, V23, 1	test instruction (dest is a source)	
00001E26	E760 5028 080E		00001DF0	1287+	VST	V22, V1023	save v1 output	
00001E2C	07FB			1288+	BR	R11	return	
00001E30				1289+RE23	DC	0F	xl16 expected result	
00001E30				1290+	DROP	R5		
00001E30	00010001 FFFD0001			1291	DC	XL16' 00010001FFFD000100AA80000123001F'	expected result	
00001E38	00AA8000 0123001F							
00001E40	0001FFFF FFFD8000			1292	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2	
00001E48	7FFF8000 0123001F							
00001E50	00020001 FFFE0001			1293	DC	XL16' 00020001FFFE000100AA800112340020'	v3	
00001E58	00AA8001 12340020							
				1294				
				1295 * Word				
00001E60				1296	VRR_C	VMNL, 2		
00001E60		00001E60		1297+	DS	0FD		
00001E60	00001EA0			1298+	USING	*, R5	base for test data and test routine	
				1299+T24	DC	A(X24)	address of test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00001E64	0018			1300+	DC	H' 24'
00001E66	00			1301+	DC	X' 00'
00001E67	02			1302+	DC	HL1' 2'
00001E68	E5D4D5D3 40404040			1303+	DC	CL8' VMNL'
00001E70	00001ED8			1304+	DC	A(RE24+16)
00001E74	00001EE8			1305+	DC	A(RE24+32)
00001E78	00000010			1306+	DC	A(16)
00001E7C	00001EC8			1307+REA24	DC	A(RE24)
00001E80	00000000 00000000			1308+	DS	FD
00001E88	00000000 00000000			1309+V1024	DS	XL16
00001E90	00000000 00000000					
00001E98	00000000 00000000			1310+	DS	FD
				1311+*		gap
00001EA0				1312+X24	DS	0F
00001EA0	E310 5010 0014		00000010	1313+	LGF	R1, V2ADDR
00001EA6	E761 0000 0806		00000000	1314+	VL	v22, 0(R1)
00001EAC	E310 5014 0014		00000014	1315+	LGF	R1, V3ADDR
00001EB2	E771 0000 0806		00000000	1316+	VL	v23, 0(R1)
00001EB8	E766 7000 2EFC			1317+	VMNL	V22, V22, V23, 2
00001EBE	E760 5028 080E		00001E88	1318+	VST	V22, V1024
00001EC4	07FB			1319+	BR	R11
00001EC8				1320+RE24	DC	0F
00001EC8				1321+	DROP	R5
00001EC8	FFFFFFFFE 0000000A			1322	DC	XL16' FFFFFFFFE0000000A012345670000001F'
00001ED0	01234567 0000001F					expected result
00001ED8	FFFFFFFFF 7FFFFFFFF			1323	DC	XL16' FFFFFFFF7FFFFFFFF012345670000001F'
00001EE0	01234567 0000001F					v2
00001EE8	FFFFFFFFE 0000000A			1324	DC	XL16' FFFFFFFFE0000000A1234567800000020'
00001EF0	12345678 00000020					v3
				1325		
				1326 * Doubleword		
				1327	VRR_C	VMNL, 3
00001EF8				1328+	DS	0FD
00001EF8		00001EF8		1329+	USING	*, R5
00001EF8	00001F38			1330+T25	DC	A(X25)
00001EFC	0019			1331+	DC	H' 25'
00001EFE	00			1332+	DC	X' 00'
00001EFF	03			1333+	DC	HL1' 3'
00001F00	E5D4D5D3 40404040			1334+	DC	CL8' VMNL'
00001F08	00001F70			1335+	DC	A(RE25+16)
00001F0C	00001F80			1336+	DC	A(RE25+32)
00001F10	00000010			1337+	DC	A(16)
00001F14	00001F60			1338+REA25	DC	A(RE25)
00001F18	00000000 00000000			1339+	DS	FD
00001F20	00000000 00000000			1340+V1025	DS	XL16
00001F28	00000000 00000000					gap
00001F30	00000000 00000000			1341+	DS	FD
				1342+*		gap
00001F38				1343+X25	DS	0F
00001F38	E310 5010 0014		00000010	1344+	LGF	R1, V2ADDR
00001F3E	E761 0000 0806		00000000	1345+	VL	v22, 0(R1)
00001F44	E310 5014 0014		00000014	1346+	LGF	R1, V3ADDR
00001F4A	E771 0000 0806		00000000	1347+	VL	v23, 0(R1)
00001F50	E766 7000 3EFC			1348+	VMNL	V22, V22, V23, 3
00001F56	E760 5028 080E		00001F20	1349+	VST	V22, V1025
00001F5C	07FB			1350+	BR	R11
						return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001F60				1351+RE25	DC	0F	xl16 expected result
00001F60				1352+	DROP	R5	
00001F60	FFFFFFFF FFFFFFFFD			1353	DC	XL16' FFFFFFFFFFFFFFFFFFD000000000000001F'	expected result
00001F68	00000000 0000001F						
00001F70	FFFFFFFF FFFFFFFF			1354	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
00001F78	00000000 0000001F						
00001F80	FFFFFFFF FFFFFFFFD			1355	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	v3
00001F88	00000000 00000020						
				1356			
				1357 * quadword			
				1358	VRR_C	VMNL, 4	
00001F90				1359+	DS	0FD	
00001F90		00001F90		1360+	USING	*, R5	base for test data and test routine
00001F90	00001FD0			1361+T26	DC	A(X26)	address of test routine
00001F94	001A			1362+	DC	H' 26'	test number
00001F96	00			1363+	DC	X' 00'	
00001F97	04			1364+	DC	HL1' 4'	m4
00001F98	E5D4D5D3 40404040			1365+	DC	CL8' VMNL'	instruction name
00001FA0	00002008			1366+	DC	A(RE26+16)	address of v2 source
00001FA4	00002018			1367+	DC	A(RE26+32)	address of v3 source
00001FA8	00000010			1368+	DC	A(16)	result length
00001FAC	00001FF8			1369+REA26	DC	A(RE26)	result address
00001FB0	00000000 00000000			1370+	DS	FD	gap
00001FB8	00000000 00000000			1371+V1026	DS	XL16	V1 output
00001FC0	00000000 00000000						
00001FC8	00000000 00000000			1372+	DS	FD	gap
				1373+*			
00001FD0				1374+X26	DS	0F	
00001FD0	E310 5010 0014		00000010	1375+	LGF	R1, V2ADDR	load v2 source
00001FD6	E761 0000 0806		00000000	1376+	VL	v22, 0(R1)	use v22 to test decoder
00001FDC	E310 5014 0014		00000014	1377+	LGF	R1, V3ADDR	load v3 source
00001FE2	E771 0000 0806		00000000	1378+	VL	v23, 0(R1)	use v23 to test decoder
00001FE8	E766 7000 4EFC			1379+	VMNL	V22, V22, V23, 4	test instruction (dest is a source)
00001FEE	E760 5028 080E		00001FB8	1380+	VST	V22, V1026	save v1 output
00001FF4	07FB			1381+	BR	R11	return
00001FF8				1382+RE26	DC	0F	xl16 expected result
00001FF8				1383+	DROP	R5	
00001FF8	FFFFFFFF FFFFFFFFD			1384	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	expected result
00002000	00000000 00000020						
00002008	FFFFFFFF FFFFFFFF			1385	DC	XL16' FFFFFFFFFFFFFFFFFF000000000000001F'	v2
00002010	00000000 0000001F						
00002018	FFFFFFFF FFFFFFFFD			1386	DC	XL16' FFFFFFFFFFFFFFFFFFD0000000000000020'	v3
00002020	00000000 00000020						
				1387			
				1388 * quadword			
				1389	VRR_C	VMNL, 4	
00002028				1390+	DS	0FD	
00002028		00002028		1391+	USING	*, R5	base for test data and test routine
00002028	00002068			1392+T27	DC	A(X27)	address of test routine
0000202C	001B			1393+	DC	H' 27'	test number
0000202E	00			1394+	DC	X' 00'	
0000202F	04			1395+	DC	HL1' 4'	m4
00002030	E5D4D5D3 40404040			1396+	DC	CL8' VMNL'	instruction name
00002038	000020A0			1397+	DC	A(RE27+16)	address of v2 source
0000203C	000020B0			1398+	DC	A(RE27+32)	address of v3 source
00002040	00000010			1399+	DC	A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002044	00002090			1400+REA27	DC	A(RE27)	result address
00002048	00000000 00000000			1401+	DS	FD	gap
00002050	00000000 00000000			1402+V1027	DS	XL16	V1 output
00002058	00000000 00000000						
00002060	00000000 00000000			1403+	DS	FD	gap
				1404+*			
00002068				1405+X27	DS	OF	
00002068	E310 5010 0014		00000010	1406+	LGF	R1, V2ADDR	load v2 source
0000206E	E761 0000 0806		00000000	1407+	VL	v22, 0(R1)	use v22 to test decoder
00002074	E310 5014 0014		00000014	1408+	LGF	R1, V3ADDR	load v3 source
0000207A	E771 0000 0806		00000000	1409+	VL	v23, 0(R1)	use v23 to test decoder
00002080	E766 7000 4EFC			1410+	VMNL	V22, V22, V23, 4	test instruction (dest is a source)
00002086	E760 5028 080E		00002050	1411+	VST	V22, V1027	save v1 output
0000208C	07FB			1412+	BR	R11	return
00002090				1413+RE27	DC	OF	xl16 expected result
00002090				1414+	DROP	R5	
00002090	0001FFFF FFFD8000			1415	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	expected result
00002098	7FFF8000 0123001F						
000020A0	0001FFFF FFFD8000			1416	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
000020A8	7FFF8000 0123001F						
000020B0	FFFFFFFF FFFFFFFD			1417	DC	XL16' FFFFFFFFFFFFFFFFD0000000000000020'	v3
000020B8	00000000 00000020						
				1418			
				1419 * quadword			
000020C0				1420	VRR_C	VMNL, 4	
000020C0		000020C0		1421+	DS	OFD	
000020C0	00002100			1422+	USING	*, R5	base for test data and test routine
000020C4	001C			1423+T28	DC	A(X28)	address of test routine
000020C6	00			1424+	DC	H' 28'	test number
000020C7	04			1425+	DC	X' 00'	
000020C8	E5D4D5D3 40404040			1426+	DC	HL1' 4'	m4
000020D0	00002138			1427+	DC	CL8' VMNL'	instruction name
000020D4	00002148			1428+	DC	A(RE28+16)	address of v2 source
000020D8	00000010			1429+	DC	A(RE28+32)	address of v3 source
000020DC	00002128			1430+	DC	A(16)	result length
000020E0	00000000 00000000			1431+REA28	DC	A(RE28)	result address
000020E8	00000000 00000000			1432+	DS	FD	gap
000020F0	00000000 00000000			1433+V1028	DS	XL16	V1 output
000020F8	00000000 00000000			1434+	DS	FD	gap
				1435+*			
00002100				1436+X28	DS	OF	
00002100	E310 5010 0014		00000010	1437+	LGF	R1, V2ADDR	load v2 source
00002106	E761 0000 0806		00000000	1438+	VL	v22, 0(R1)	use v22 to test decoder
0000210C	E310 5014 0014		00000014	1439+	LGF	R1, V3ADDR	load v3 source
00002112	E771 0000 0806		00000000	1440+	VL	v23, 0(R1)	use v23 to test decoder
00002118	E766 7000 4EFC			1441+	VMNL	V22, V22, V23, 4	test instruction (dest is a source)
0000211E	E760 5028 080E		000020E8	1442+	VST	V22, V1028	save v1 output
00002124	07FB			1443+	BR	R11	return
00002128				1444+RE28	DC	OF	xl16 expected result
00002128				1445+	DROP	R5	
00002128	0001FFFF FFFD8000			1446	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	expected result
00002130	7FFF8000 0123001F						
00002138	0001FFFF FFFD8000			1447	DC	XL16' 0001FFFFFFFFFD80007FFF80000123001F'	v2
00002140	7FFF8000 0123001F						
00002148	00020001 FFFE0001			1448	DC	XL16' 00020001FFFE000100AA800112340020'	v3

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002150	00AA8001 12340020			1449		
				1450 *	-----	
				1451 * VAVG	- VECTOR AVERAGE	
				1452 *	-----	
				1453 * Byte		
00002158				1454	VRR_C VAVG, 0	
00002158		00002158		1455+	DS OFD	
00002158	00002198			1456+	USING *, R5	base for test data and test routine
0000215C	001D			1457+T29	DC A(X29)	address of test routine
0000215E	00			1458+	DC H' 29'	test number
0000215F	00			1459+	DC X' 00'	
00002160	E5C1E5C7 40404040			1460+	DC HL1' 0'	m4
00002168	000021D0			1461+	DC CL8' VAVG'	instruction name
0000216C	000021E0			1462+	DC A(RE29+16)	address of v2 source
00002170	00000010			1463+	DC A(RE29+32)	address of v3 source
00002174	000021C0			1464+	DC A(16)	result length
00002178	00000000 00000000			1465+REA29	DC A(RE29)	result address
00002180	00000000 00000000			1466+	DS FD	gap
00002188	00000000 00000000			1467+V1029	DS XL16	V1 output
00002190	00000000 00000000			1468+	DS FD	gap
				1469+*		
00002198				1470+X29	DS OF	
00002198	E310 5010 0014		00000010	1471+	LGF R1, V2ADDR	load v2 source
0000219E	E761 0000 0806		00000000	1472+	VL v22, 0(R1)	use v22 to test decoder
000021A4	E310 5014 0014		00000014	1473+	LGF R1, V3ADDR	load v3 source
000021AA	E771 0000 0806		00000000	1474+	VL v23, 0(R1)	use v23 to test decoder
000021B0	E766 7000 0EF2			1475+	VAVG V22, V22, V23, 0	test instruction (dest is a source)
000021B6	E760 5028 080E		00002180	1476+	VST V22, V1029	save v1 output
000021BC	07FB			1477+	BR R11	return
000021C0				1478+RE29	DC OF	xl16 expected result
000021C0				1479+	DROP R5	
000021C0	FFFFFFFF FFFFFFFF			1480	DC XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	expected result
000021C8	FFFFFFFF FFFFFFFF					
000021D0	7C7C7C7C 7C7C7C7C			1481	DC XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
000021D8	7C7C7C7C 7C7C7C7C					
000021E0	82828282 82828282			1482	DC XL16' 828282828282828282828282828282'	v3
000021E8	82828282 82828282					
				1483		
				1484 * Hal fword		
000021F0				1485	VRR_C VAVG, 1	
000021F0		000021F0		1486+	DS OFD	
000021F0	00002230			1487+	USING *, R5	base for test data and test routine
000021F4	001E			1488+T30	DC A(X30)	address of test routine
000021F6	00			1489+	DC H' 30'	test number
000021F7	01			1490+	DC X' 00'	
000021F8	E5C1E5C7 40404040			1491+	DC HL1' 1'	m4
00002200	00002268			1492+	DC CL8' VAVG'	instruction name
00002204	00002278			1493+	DC A(RE30+16)	address of v2 source
00002208	00000010			1494+	DC A(RE30+32)	address of v3 source
0000220C	00002258			1495+	DC A(16)	result length
00002210	00000000 00000000			1496+REA30	DC A(RE30)	result address
00002218	00000000 00000000			1497+	DS FD	gap
00002220	00000000 00000000			1498+V1030	DS XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002228	00000000 00000000			1499+ 1500+*	DS	FD	gap
00002230				1501+X30	DS	OF	
00002230	E310 5010 0014		00000010	1502+	LGF	R1, V2ADDR	load v2 source
00002236	E761 0000 0806		00000000	1503+	VL	v22, 0(R1)	use v22 to test decoder
0000223C	E310 5014 0014		00000014	1504+	LGF	R1, V3ADDR	load v3 source
00002242	E771 0000 0806		00000000	1505+	VL	v23, 0(R1)	use v23 to test decoder
00002248	E766 7000 1EF2			1506+	VAVG	V22, V22, V23, 1	test instruction (dest is a source)
0000224E	E760 A018 080E		00002218	1507+	VST	V22, V1030	save v1 output
00002254	07FB			1508+	BR	R11	return
00002258				1509+RE30	DC	OF	xl16 expected result
00002258				1510+	DROP	R5	
00002258	FF7FFF7F FF7FFF7F			1511	DC	XL16' FF7FFF7FFF7FFF7FFF7FFF7FFF7FFF7F'	expected result
00002260	FF7FFF7F FF7FFF7F						
00002268	7C7C7C7C 7C7C7C7C			1512	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002270	7C7C7C7C 7C7C7C7C						
00002278	82828282 82828282			1513	DC	XL16' 82828282828282828282828282828282'	v3
00002280	82828282 82828282						
				1514			
				1515 * Word			
				1516	VRR_C	VAVG, 2	
00002288				1517+	DS	OFD	
00002288		00002288		1518+	USING	*, R5	base for test data and test routine
00002288	000022C8			1519+T31	DC	A(X31)	address of test routine
0000228C	001F			1520+	DC	H' 31'	test number
0000228E	00			1521+	DC	X' 00'	
0000228F	02			1522+	DC	HL1' 2'	m4
00002290	E5C1E5C7 40404040			1523+	DC	CL8' VAVG'	instruction name
00002298	00002300			1524+	DC	A(RE31+16)	address of v2 source
0000229C	00002310			1525+	DC	A(RE31+32)	address of v3 source
000022A0	00000010			1526+	DC	A(16)	result length
000022A4	000022F0			1527+REA31	DC	A(RE31)	result address
000022A8	00000000 00000000			1528+	DS	FD	gap
000022B0	00000000 00000000			1529+V1031	DS	XL16	V1 output
000022B8	00000000 00000000						
000022C0	00000000 00000000			1530+	DS	FD	gap
				1531+*			
000022C8				1532+X31	DS	OF	
000022C8	E310 5010 0014		00000010	1533+	LGF	R1, V2ADDR	load v2 source
000022CE	E761 0000 0806		00000000	1534+	VL	v22, 0(R1)	use v22 to test decoder
000022D4	E310 5014 0014		00000014	1535+	LGF	R1, V3ADDR	load v3 source
000022DA	E771 0000 0806		00000000	1536+	VL	v23, 0(R1)	use v23 to test decoder
000022E0	E766 7000 2EF2			1537+	VAVG	V22, V22, V23, 2	test instruction (dest is a source)
000022E6	E760 5028 080E		000022B0	1538+	VST	V22, V1031	save v1 output
000022EC	07FB			1539+	BR	R11	return
000022F0				1540+RE31	DC	OF	xl16 expected result
000022F0				1541+	DROP	R5	
000022F0	FF7F7F7F FF7F7F7F			1542	DC	XL16' FF7F7F7FFF7F7F7FFF7F7F7FFF7F7F7F'	expected result
000022F8	FF7F7F7F FF7F7F7F						
00002300	7C7C7C7C 7C7C7C7C			1543	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002308	7C7C7C7C 7C7C7C7C						
00002310	82828282 82828282			1544	DC	XL16' 82828282828282828282828282828282'	v3
00002318	82828282 82828282						
				1545			
				1546 * Doubleword			
				1547	VRR_C	VAVG, 3	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
00002320				1548+	DS	OFD
00002320		00002320		1549+	USING	*, R5
00002320	00002360			1550+T32	DC	A(X32)
00002324	0020			1551+	DC	H' 32'
00002326	00			1552+	DC	X' 00'
00002327	03			1553+	DC	HL1' 3'
00002328	E5C1E5C7 40404040			1554+	DC	CL8' VAVG'
00002330	00002398			1555+	DC	A(RE32+16)
00002334	000023A8			1556+	DC	A(RE32+32)
00002338	00000010			1557+	DC	A(16)
0000233C	00002388			1558+REA32	DC	A(RE32)
00002340	00000000 00000000			1559+	DS	FD
00002348	00000000 00000000			1560+V1032	DS	XL16
00002350	00000000 00000000					
00002358	00000000 00000000			1561+	DS	FD
				1562+*		gap
00002360				1563+X32	DS	OF
00002360	E310 5010 0014		00000010	1564+	LGF	R1, V2ADDR
00002366	E761 0000 0806		00000000	1565+	VL	v22, 0(R1)
0000236C	E310 5014 0014		00000014	1566+	LGF	R1, V3ADDR
00002372	E771 0000 0806		00000000	1567+	VL	v23, 0(R1)
00002378	E766 7000 3EF2			1568+	VAVG	V22, V22, V23, 3
0000237E	E760 5028 080E		00002348	1569+	VST	V22, V1032
00002384	07FB			1570+	BR	R11
00002388				1571+RE32	DC	OF
00002388				1572+	DROP	R5
00002388	FF7F7F7F 7F7F7F7F			1573	DC	XL16' FF7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'
00002390	FF7F7F7F 7F7F7F7F					expected result
00002398	7C7C7C7C 7C7C7C7C			1574	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'
000023A0	7C7C7C7C 7C7C7C7C					v2
000023A8	82828282 82828282			1575	DC	XL16' 82828282828282828282828282828282'
000023B0	82828282 82828282					v3
				1576		
				1577 * Doubleword		
				1578	VRR_C	VAVG, 3
000023B8				1579+	DS	OFD
000023B8		000023B8		1580+	USING	*, R5
000023B8	000023F8			1581+T33	DC	A(X33)
000023BC	0021			1582+	DC	H' 33'
000023BE	00			1583+	DC	X' 00'
000023BF	03			1584+	DC	HL1' 3'
000023C0	E5C1E5C7 40404040			1585+	DC	CL8' VAVG'
000023C8	00002430			1586+	DC	A(RE33+16)
000023CC	00002440			1587+	DC	A(RE33+32)
000023D0	00000010			1588+	DC	A(16)
000023D4	00002420			1589+REA33	DC	A(RE33)
000023D8	00000000 00000000			1590+	DS	FD
000023E0	00000000 00000000			1591+V1033	DS	XL16
000023E8	00000000 00000000					
000023F0	00000000 00000000			1592+	DS	FD
				1593+*		gap
000023F8				1594+X33	DS	OF
000023F8	E310 5010 0014		00000010	1595+	LGF	R1, V2ADDR
000023FE	E761 0000 0806		00000000	1596+	VL	v22, 0(R1)
00002404	E310 5014 0014		00000014	1597+	LGF	R1, V3ADDR
0000240A	E771 0000 0806		00000000	1598+	VL	v23, 0(R1)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002410	E766 7000 3EF2			1599+	VAVG	V22, V22, V23, 3	test instruction (dest is a source)
00002416	E760 5028 080E		000023E0	1600+	VST	V22, V1033	save v1 output
0000241C	07FB			1601+	BR	R11	return
00002420				1602+RE33	DC	0F	xl16 expected result
00002420				1603+	DROP	R5	
00002420	7FFFFFFF FFFFFFFFC			1604	DC	XL16' 7FFFFFFF7FFFFFFFC7FFFFFFF7FFFFFFFC'	expected result
00002428	7FFFFFFF FFFFFFFFC						
00002430	7FFFFFFF FFFFFFFFC			1605	DC	XL16' 7FFFFFFF7FFFFFFFC7FFFFFFF7FFFFFFFC'	v2
00002438	7FFFFFFF FFFFFFFFC						
00002440	7FFFFFFF FFFFFFFFC			1606	DC	XL16' 7FFFFFFF7FFFFFFFC7FFFFFFF7FFFFFFFC'	v3
00002448	7FFFFFFF FFFFFFFFC						
				1607			
				1608 * Doubleword			
				1609	VRR_C	VAVG, 3	
00002450				1610+	DS	0FD	
00002450		00002450		1611+	USING	*, R5	base for test data and test routine
00002450	00002490			1612+T34	DC	A(X34)	address of test routine
00002454	0022			1613+	DC	H' 34'	test number
00002456	00			1614+	DC	X' 00'	
00002457	03			1615+	DC	HL1' 3'	m4
00002458	E5C1E5C7 40404040			1616+	DC	CL8' VAVG'	instruction name
00002460	000024C8			1617+	DC	A(RE34+16)	address of v2 source
00002464	000024D8			1618+	DC	A(RE34+32)	address of v3 source
00002468	00000010			1619+	DC	A(16)	result length
0000246C	000024B8			1620+REA34	DC	A(RE34)	result address
00002470	00000000 00000000			1621+	DS	FD	gap
00002478	00000000 00000000			1622+V1034	DS	XL16	V1 output
00002480	00000000 00000000						
00002488	00000000 00000000			1623+	DS	FD	gap
				1624+*			
00002490				1625+X34	DS	0F	
00002490	E310 5010 0014		00000010	1626+	LGF	R1, V2ADDR	load v2 source
00002496	E761 0000 0806		00000000	1627+	VL	v22, 0(R1)	use v22 to test decoder
0000249C	E310 5014 0014		00000014	1628+	LGF	R1, V3ADDR	load v3 source
000024A2	E771 0000 0806		00000000	1629+	VL	v23, 0(R1)	use v23 to test decoder
000024A8	E766 7000 3EF2			1630+	VAVG	V22, V22, V23, 3	test instruction (dest is a source)
000024AE	E760 5028 080E		00002478	1631+	VST	V22, V1034	save v1 output
000024B4	07FB			1632+	BR	R11	return
000024B8				1633+RE34	DC	0F	xl16 expected result
000024B8				1634+	DROP	R5	
000024B8	FFFFFFFF FFFFFFFF			1635	DC	XL16' FFFFFFFF7FFFFFFFC7FFFFFFF7FFFFFFFC'	expected result
000024C0	FFFFFFFF FFFFFFFF						
000024C8	80000000 00000002			1636	DC	XL16' 80000000000000028000000000000002'	v2
000024D0	80000000 00000002						
000024D8	7FFFFFFF FFFFFFFFC			1637	DC	XL16' 7FFFFFFF7FFFFFFFC7FFFFFFF7FFFFFFFC'	v3
000024E0	7FFFFFFF FFFFFFFFC						
				1638			
				1639 * Doubleword			
				1640	VRR_C	VAVG, 3	
000024E8				1641+	DS	0FD	
000024E8		000024E8		1642+	USING	*, R5	base for test data and test routine
000024E8	00002528			1643+T35	DC	A(X35)	address of test routine
000024EC	0023			1644+	DC	H' 35'	test number
000024EE	00			1645+	DC	X' 00'	
000024EF	03			1646+	DC	HL1' 3'	m4
000024F0	E5C1E5C7 40404040			1647+	DC	CL8' VAVG'	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000024F8	00002560			1648+	DC	A(RE35+16)	address of v2 source
000024FC	00002570			1649+	DC	A(RE35+32)	address of v3 source
00002500	00000010			1650+	DC	A(16)	result length
00002504	00002550			1651+REA35	DC	A(RE35)	result address
00002508	00000000 00000000			1652+	DS	FD	gap
00002510	00000000 00000000			1653+V1035	DS	XL16	V1 output
00002518	00000000 00000000						
00002520	00000000 00000000			1654+	DS	FD	gap
				1655+*			
00002528				1656+X35	DS	OF	
00002528	E310 5010 0014		00000010	1657+	LGF	R1, V2ADDR	load v2 source
0000252E	E761 0000 0806		00000000	1658+	VL	v22, 0(R1)	use v22 to test decoder
00002534	E310 5014 0014		00000014	1659+	LGF	R1, V3ADDR	load v3 source
0000253A	E771 0000 0806		00000000	1660+	VL	v23, 0(R1)	use v23 to test decoder
00002540	E766 7000 3EF2			1661+	VAVG	V22, V22, V23, 3	test instruction (dest is a source)
00002546	E760 5028 080E		00002510	1662+	VST	V22, V1035	save v1 output
0000254C	07FB			1663+	BR	R11	return
00002550				1664+RE35	DC	OF	xl16 expected result
00002550				1665+	DROP	R5	
00002550	FFFFFFFF FFFFFFFF			1666	DC	XL16' FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF'	expected result
00002558	FFFFFFFF FFFFFFFF						
00002560	7FFFFFFFF FFFFFFFFC			1667	DC	XL16' 7FFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFC'	v2
00002568	7FFFFFFFF FFFFFFFFC						
00002570	80000000 00000002			1668	DC	XL16' 8000000000000002800000000000002'	v3
00002578	80000000 00000002						
				1669			
				1670 * Doubleword			
				1671	VRR_C	VAVG, 3	
00002580				1672+	DS	OFD	
00002580		00002580		1673+	USING	*, R5	base for test data and test routine
00002580	000025C0			1674+T36	DC	A(X36)	address of test routine
00002584	0024			1675+	DC	H' 36'	test number
00002586	00			1676+	DC	X' 00'	
00002587	03			1677+	DC	HL1' 3'	m4
00002588	E5C1E5C7 40404040			1678+	DC	CL8' VAVG'	instruction name
00002590	000025F8			1679+	DC	A(RE36+16)	address of v2 source
00002594	00002608			1680+	DC	A(RE36+32)	address of v3 source
00002598	00000010			1681+	DC	A(16)	result length
0000259C	000025E8			1682+REA36	DC	A(RE36)	result address
000025A0	00000000 00000000			1683+	DS	FD	gap
000025A8	00000000 00000000			1684+V1036	DS	XL16	V1 output
000025B0	00000000 00000000						
000025B8	00000000 00000000			1685+	DS	FD	gap
				1686+*			
000025C0				1687+X36	DS	OF	
000025C0	E310 5010 0014		00000010	1688+	LGF	R1, V2ADDR	load v2 source
000025C6	E761 0000 0806		00000000	1689+	VL	v22, 0(R1)	use v22 to test decoder
000025CC	E310 5014 0014		00000014	1690+	LGF	R1, V3ADDR	load v3 source
000025D2	E771 0000 0806		00000000	1691+	VL	v23, 0(R1)	use v23 to test decoder
000025D8	E766 7000 3EF2			1692+	VAVG	V22, V22, V23, 3	test instruction (dest is a source)
000025DE	E760 5028 080E		000025A8	1693+	VST	V22, V1036	save v1 output
000025E4	07FB			1694+	BR	R11	return
000025E8				1695+RE36	DC	OF	xl16 expected result
000025E8				1696+	DROP	R5	
000025E8	80000000 00000002			1697	DC	XL16' 8000000000000002800000000000002'	expected result
000025F0	80000000 00000002						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000025F8	80000000 00000002			1698	DC	XL16' 80000000000000002800000000000002'	v2
00002600	80000000 00000002						
00002608	80000000 00000002			1699	DC	XL16' 80000000000000002800000000000002'	v3
00002610	80000000 00000002						
				1700			
				1701 * Quadword			
				1702	VRR_C	VAVG, 4	
00002618				1703+	DS	OFD	
00002618		00002618		1704+	USING	*, R5	base for test data and test routine
00002618	00002658			1705+T37	DC	A(X37)	address of test routine
0000261C	0025			1706+	DC	H' 37'	test number
0000261E	00			1707+	DC	X' 00'	
0000261F	04			1708+	DC	HL1' 4'	m4
00002620	E5C1E5C7 40404040			1709+	DC	CL8' VAVG'	instruction name
00002628	00002690			1710+	DC	A(RE37+16)	address of v2 source
0000262C	000026A0			1711+	DC	A(RE37+32)	address of v3 source
00002630	00000010			1712+	DC	A(16)	result length
00002634	00002680			1713+REA37	DC	A(RE37)	result address
00002638	00000000 00000000			1714+	DS	FD	gap
00002640	00000000 00000000			1715+V1037	DS	XL16	V1 output
00002648	00000000 00000000						
00002650	00000000 00000000			1716+	DS	FD	gap
				1717+*			
00002658				1718+X37	DS	OF	
00002658	E310 5010 0014		00000010	1719+	LGF	R1, V2ADDR	load v2 source
0000265E	E761 0000 0806		00000000	1720+	VL	v22, 0(R1)	use v22 to test decoder
00002664	E310 5014 0014		00000014	1721+	LGF	R1, V3ADDR	load v3 source
0000266A	E771 0000 0806		00000000	1722+	VL	v23, 0(R1)	use v23 to test decoder
00002670	E766 7000 4EF2			1723+	VAVG	V22, V22, V23, 4	test instruction (dest is a source)
00002676	E760 5028 080E		00002640	1724+	VST	V22, V1037	save v1 output
0000267C	07FB			1725+	BR	R11	return
00002680				1726+RE37	DC	OF	xl16 expected result
00002680				1727+	DROP	R5	
00002680	7F7F7F7F 7F7F7F7F			1728	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002688	7F7F7F7F 7F7F7F7F						
00002690	7C7C7C7C 7C7C7C7C			1729	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002698	7C7C7C7C 7C7C7C7C						
000026A0	82828282 82828282			1730	DC	XL16' 828282828282828282828282828282'	v3
000026A8	82828282 82828282						
				1731			
				1732 * Quadword			
				1733	VRR_C	VAVG, 4	
000026B0				1734+	DS	OFD	
000026B0		000026B0		1735+	USING	*, R5	base for test data and test routine
000026B0	000026F0			1736+T38	DC	A(X38)	address of test routine
000026B4	0026			1737+	DC	H' 38'	test number
000026B6	00			1738+	DC	X' 00'	
000026B7	04			1739+	DC	HL1' 4'	m4
000026B8	E5C1E5C7 40404040			1740+	DC	CL8' VAVG'	instruction name
000026C0	00002728			1741+	DC	A(RE38+16)	address of v2 source
000026C4	00002738			1742+	DC	A(RE38+32)	address of v3 source
000026C8	00000010			1743+	DC	A(16)	result length
000026CC	00002718			1744+REA38	DC	A(RE38)	result address
000026D0	00000000 00000000			1745+	DS	FD	gap
000026D8	00000000 00000000			1746+V1038	DS	XL16	V1 output
000026E0	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000026E8	00000000 00000000			1747+ 1748+*	DS	FD	gap
000026F0				1749+X38	DS	0F	
000026F0	E310 5010 0014		00000010	1750+	LGF	R1, V2ADDR	load v2 source
000026F6	E761 0000 0806		00000000	1751+	VL	v22, 0(R1)	use v22 to test decoder
000026FC	E310 5014 0014		00000014	1752+	LGF	R1, V3ADDR	load v3 source
00002702	E771 0000 0806		00000000	1753+	VL	v23, 0(R1)	use v23 to test decoder
00002708	E766 7000 4EF2			1754+	VAVG	V22, V22, V23, 4	test instruction (dest is a source)
0000270E	E760 5028 080E		000026D8	1755+	VST	V22, V1038	save v1 output
00002714	07FB			1756+	BR	R11	return
00002718				1757+RE38	DC	0F	xl16 expected result
00002718				1758+	DROP	R5	
00002718	7FFFFFFF FFFFFFFC			1759	DC	XL16' 7FFFFFFF7FFFFFFF'	expected result
00002720	7FFFFFFF FFFFFFFC						
00002728	7FFFFFFF FFFFFFFC			1760	DC	XL16' 7FFFFFFF7FFFFFFF'	v2
00002730	7FFFFFFF FFFFFFFC						
00002738	7FFFFFFF FFFFFFFC			1761	DC	XL16' 7FFFFFFF7FFFFFFF'	v3
00002740	7FFFFFFF FFFFFFFC						
				1762			
				1763 * Quadword			
				1764	VRR_C	VAVG, 4	
00002748				1765+	DS	0FD	
00002748		00002748		1766+	USING	*, R5	base for test data and test routine
00002748	00002788			1767+T39	DC	A(X39)	address of test routine
0000274C	0027			1768+	DC	H' 39'	test number
0000274E	00			1769+	DC	X' 00'	
0000274F	04			1770+	DC	HL1' 4'	m4
00002750	E5C1E5C7 40404040			1771+	DC	CL8' VAVG'	instruction name
00002758	000027C0			1772+	DC	A(RE39+16)	address of v2 source
0000275C	000027D0			1773+	DC	A(RE39+32)	address of v3 source
00002760	00000010			1774+	DC	A(16)	result length
00002764	000027B0			1775+REA39	DC	A(RE39)	result address
00002768	00000000 00000000			1776+	DS	FD	gap
00002770	00000000 00000000			1777+V1039	DS	XL16	V1 output
00002778	00000000 00000000						
00002780	00000000 00000000			1778+	DS	FD	gap
				1779+*			
00002788				1780+X39	DS	0F	
00002788	E310 5010 0014		00000010	1781+	LGF	R1, V2ADDR	load v2 source
0000278E	E761 0000 0806		00000000	1782+	VL	v22, 0(R1)	use v22 to test decoder
00002794	E310 5014 0014		00000014	1783+	LGF	R1, V3ADDR	load v3 source
0000279A	E771 0000 0806		00000000	1784+	VL	v23, 0(R1)	use v23 to test decoder
000027A0	E766 7000 4EF2			1785+	VAVG	V22, V22, V23, 4	test instruction (dest is a source)
000027A6	E760 5028 080E		00002770	1786+	VST	V22, V1039	save v1 output
000027AC	07FB			1787+	BR	R11	return
000027B0				1788+RE39	DC	0F	xl16 expected result
000027B0				1789+	DROP	R5	
000027B0	7FFFFFFF FFFFFFFF			1790	DC	XL16' 7FFFFFFF7FFFFFFF'	expected result
000027B8	7FFFFFFF FFFFFFFF						
000027C0	80000000 00000002			1791	DC	XL16' 80000000000000028000000000000002'	v2
000027C8	80000000 00000002						
000027D0	7FFFFFFF FFFFFFFC			1792	DC	XL16' 7FFFFFFF7FFFFFFF'	v3
000027D8	7FFFFFFF FFFFFFFC						
				1793			
				1794 * Quadword			
				1795	VRR_C	VAVG, 4	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000027E0				1796+	DS	0FD	
000027E0		000027E0		1797+	USING	*, R5	base for test data and test routine
000027E0	00002820			1798+T40	DC	A(X40)	address of test routine
000027E4	0028			1799+	DC	H' 40'	test number
000027E6	00			1800+	DC	X' 00'	
000027E7	04			1801+	DC	HL1' 4'	m4
000027E8	E5C1E5C7 40404040			1802+	DC	CL8' VAVG'	instruction name
000027F0	00002858			1803+	DC	A(RE40+16)	address of v2 source
000027F4	00002868			1804+	DC	A(RE40+32)	address of v3 source
000027F8	00000010			1805+	DC	A(16)	result length
000027FC	00002848			1806+REA40	DC	A(RE40)	result address
00002800	00000000 00000000			1807+	DS	FD	gap
00002808	00000000 00000000			1808+V1040	DS	XL16	V1 output
00002810	00000000 00000000						
00002818	00000000 00000000			1809+	DS	FD	gap
				1810+*			
00002820				1811+X40	DS	0F	
00002820	E310 5010 0014		00000010	1812+	LGF	R1, V2ADDR	load v2 source
00002826	E761 0000 0806		00000000	1813+	VL	v22, 0(R1)	use v22 to test decoder
0000282C	E310 5014 0014		00000014	1814+	LGF	R1, V3ADDR	load v3 source
00002832	E771 0000 0806		00000000	1815+	VL	v23, 0(R1)	use v23 to test decoder
00002838	E766 7000 4EF2			1816+	VAVG	V22, V22, V23, 4	test instruction (dest is a source)
0000283E	E760 5028 080E		00002808	1817+	VST	V22, V1040	save v1 output
00002844	07FB			1818+	BR	R11	return
00002848				1819+RE40	DC	0F	xl16 expected result
00002848				1820+	DROP	R5	
00002848	7FFFFFFF FFFFFFFF			1821	DC	XL16' 7FFFFFFF7FFFFFFF7FFFFFFF7FFFFFFF'	expected result
00002850	7FFFFFFF FFFFFFFF						
00002858	7FFFFFFF FFFFFFFFC			1822	DC	XL16' 7FFFFFFFC7FFFFFFFC'	v2
00002860	7FFFFFFF FFFFFFFFC						
00002868	80000000 00000002			1823	DC	XL16' 8000000000000002800000000000002'	v3
00002870	80000000 00000002						
				1824			
				1825 * Quadword			
				1826	VRR_C	VAVG, 4	
00002878				1827+	DS	0FD	
00002878		00002878		1828+	USING	*, R5	base for test data and test routine
00002878	000028B8			1829+T41	DC	A(X41)	address of test routine
0000287C	0029			1830+	DC	H' 41'	test number
0000287E	00			1831+	DC	X' 00'	
0000287F	04			1832+	DC	HL1' 4'	m4
00002880	E5C1E5C7 40404040			1833+	DC	CL8' VAVG'	instruction name
00002888	000028F0			1834+	DC	A(RE41+16)	address of v2 source
0000288C	00002900			1835+	DC	A(RE41+32)	address of v3 source
00002890	00000010			1836+	DC	A(16)	result length
00002894	000028E0			1837+REA41	DC	A(RE41)	result address
00002898	00000000 00000000			1838+	DS	FD	gap
000028A0	00000000 00000000			1839+V1041	DS	XL16	V1 output
000028A8	00000000 00000000						
000028B0	00000000 00000000			1840+	DS	FD	gap
				1841+*			
000028B8				1842+X41	DS	0F	
000028B8	E310 5010 0014		00000010	1843+	LGF	R1, V2ADDR	load v2 source
000028BE	E761 0000 0806		00000000	1844+	VL	v22, 0(R1)	use v22 to test decoder
000028C4	E310 5014 0014		00000014	1845+	LGF	R1, V3ADDR	load v3 source
000028CA	E771 0000 0806		00000000	1846+	VL	v23, 0(R1)	use v23 to test decoder

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000028D0	E766 7000 4EF2			1847+	VAVG	V22, V22, V23, 4	test instruction (dest is a source)
000028D6	E760 5028 080E		000028A0	1848+	VST	V22, V1041	save v1 output
000028DC	07FB			1849+	BR	R11	return
000028E0				1850+RE41	DC	0F	xl16 expected result
000028E0				1851+	DROP	R5	
000028E0	80000000 00000002			1852	DC	XL16' 80000000000000002800000000000002'	expected result
000028E8	80000000 00000002						
000028F0	80000000 00000002			1853	DC	XL16' 80000000000000002800000000000002'	v2
000028F8	80000000 00000002						
00002900	80000000 00000002			1854	DC	XL16' 80000000000000002800000000000002'	v3
00002908	80000000 00000002						
				1855			
				1856 *			
				1857 *VAVGL - VECTOR AVERAGE LOGICAL			
				1858 *			
				1859 * Byte			
				1860	VRR_C	VAVGL, 0	
00002910				1861+	DS	0FD	
00002910		00002910		1862+	USING	*, R5	base for test data and test routine
00002910	00002950			1863+T42	DC	A(X42)	address of test routine
00002914	002A			1864+	DC	H' 42'	test number
00002916	00			1865+	DC	X' 00'	
00002917	00			1866+	DC	HL1' 0'	m4
00002918	E5C1E5C7 D3404040			1867+	DC	CL8' VAVGL'	instruction name
00002920	00002988			1868+	DC	A(RE42+16)	address of v2 source
00002924	00002998			1869+	DC	A(RE42+32)	address of v3 source
00002928	00000010			1870+	DC	A(16)	result length
0000292C	00002978			1871+REA42	DC	A(RE42)	result address
00002930	00000000 00000000			1872+	DS	FD	gap
00002938	00000000 00000000			1873+V1042	DS	XL16	V1 output
00002940	00000000 00000000						
00002948	00000000 00000000			1874+	DS	FD	gap
				1875+*			
00002950				1876+X42	DS	0F	
00002950	E310 5010 0014		00000010	1877+	LGF	R1, V2ADDR	load v2 source
00002956	E761 0000 0806		00000000	1878+	VL	v22, 0(R1)	use v22 to test decoder
0000295C	E310 5014 0014		00000014	1879+	LGF	R1, V3ADDR	load v3 source
00002962	E771 0000 0806		00000000	1880+	VL	v23, 0(R1)	use v23 to test decoder
00002968	E766 7000 0EF0			1881+	VAVGL	V22, V22, V23, 0	test instruction (dest is a source)
0000296E	E760 5028 080E		00002938	1882+	VST	V22, V1042	save v1 output
00002974	07FB			1883+	BR	R11	return
00002978				1884+RE42	DC	0F	xl16 expected result
00002978				1885+	DROP	R5	
00002978	7F7F7F7F 7F7F7F7F			1886	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002980	7F7F7F7F 7F7F7F7F						
00002988	7C7C7C7C 7C7C7C7C			1887	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002990	7C7C7C7C 7C7C7C7C						
00002998	82828282 82828282			1888	DC	XL16' 828282828282828282828282828282'	v3
000029A0	82828282 82828282						
				1889			
				1890 * Hal fword			
				1891	VRR_C	VAVGL, 1	
000029A8				1892+	DS	0FD	
000029A8		000029A8		1893+	USING	*, R5	base for test data and test routine
000029A8	000029E8			1894+T43	DC	A(X43)	address of test routine
000029AC	002B			1895+	DC	H' 43'	test number

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000029AE	00			1896+	DC	X' 00'	
000029AF	01			1897+	DC	HL1' 1'	m4
000029B0	E5C1E5C7 D3404040			1898+	DC	CL8' VAVGL'	instruction name
000029B8	00002A20			1899+	DC	A(RE43+16)	address of v2 source
000029BC	00002A30			1900+	DC	A(RE43+32)	address of v3 source
000029C0	00000010			1901+	DC	A(16)	result length
000029C4	00002A10			1902+REA43	DC	A(RE43)	result address
000029C8	00000000 00000000			1903+	DS	FD	gap
000029D0	00000000 00000000			1904+V1043	DS	XL16	V1 output
000029D8	00000000 00000000						
000029E0	00000000 00000000			1905+	DS	FD	gap
				1906+*			
000029E8				1907+X43	DS	0F	
000029E8	E310 5010 0014		00000010	1908+	LGF	R1, V2ADDR	load v2 source
000029EE	E761 0000 0806		00000000	1909+	VL	v22, 0(R1)	use v22 to test decoder
000029F4	E310 5014 0014		00000014	1910+	LGF	R1, V3ADDR	load v3 source
000029FA	E771 0000 0806		00000000	1911+	VL	v23, 0(R1)	use v23 to test decoder
00002A00	E766 7000 1EF0			1912+	VAVGL	V22, V22, V23, 1	test instruction (dest is a source)
00002A06	E760 5028 080E		000029D0	1913+	VST	V22, V1043	save v1 output
00002A0C	07FB			1914+	BR	R11	return
00002A10				1915+RE43	DC	0F	xl16 expected result
00002A10				1916+	DROP	R5	
00002A10	7F7F7F7F 7F7F7F7F			1917	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002A18	7F7F7F7F 7F7F7F7F						
00002A20	7C7C7C7C 7C7C7C7C			1918	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002A28	7C7C7C7C 7C7C7C7C						
00002A30	82828282 82828282			1919	DC	XL16' 82828282828282828282828282828282'	v3
00002A38	82828282 82828282						
				1920			
				1921 * Word			
				1922	VRR_C	VAVGL, 2	
00002A40				1923+	DS	0FD	
00002A40		00002A40		1924+	USING	*, R5	base for test data and test routine
00002A40	00002A80			1925+T44	DC	A(X44)	address of test routine
00002A44	002C			1926+	DC	H' 44'	test number
00002A46	00			1927+	DC	X' 00'	
00002A47	02			1928+	DC	HL1' 2'	m4
00002A48	E5C1E5C7 D3404040			1929+	DC	CL8' VAVGL'	instruction name
00002A50	00002AB8			1930+	DC	A(RE44+16)	address of v2 source
00002A54	00002AC8			1931+	DC	A(RE44+32)	address of v3 source
00002A58	00000010			1932+	DC	A(16)	result length
00002A5C	00002AA8			1933+REA44	DC	A(RE44)	result address
00002A60	00000000 00000000			1934+	DS	FD	gap
00002A68	00000000 00000000			1935+V1044	DS	XL16	V1 output
00002A70	00000000 00000000						
00002A78	00000000 00000000			1936+	DS	FD	gap
				1937+*			
00002A80				1938+X44	DS	0F	
00002A80	E310 5010 0014		00000010	1939+	LGF	R1, V2ADDR	load v2 source
00002A86	E761 0000 0806		00000000	1940+	VL	v22, 0(R1)	use v22 to test decoder
00002A8C	E310 5014 0014		00000014	1941+	LGF	R1, V3ADDR	load v3 source
00002A92	E771 0000 0806		00000000	1942+	VL	v23, 0(R1)	use v23 to test decoder
00002A98	E766 7000 2EF0			1943+	VAVGL	V22, V22, V23, 2	test instruction (dest is a source)
00002A9E	E760 5028 080E		00002A68	1944+	VST	V22, V1044	save v1 output
00002AA4	07FB			1945+	BR	R11	return
00002AA8				1946+RE44	DC	0F	xl16 expected result

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002AA8				1947+	DROP	R5	
00002AA8	7F7F7F7F 7F7F7F7F			1948	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002AB0	7F7F7F7F 7F7F7F7F						
00002AB8	7C7C7C7C 7C7C7C7C			1949	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002AC0	7C7C7C7C 7C7C7C7C						
00002AC8	82828282 82828282			1950	DC	XL16' 82828282828282828282828282828282'	v3
00002AD0	82828282 82828282						
				1951			
				1952	* Doubleword		
				1953	VRR_C	VAVGL, 3	
00002AD8				1954+	DS	OFD	
00002AD8		00002AD8		1955+	USING	*, R5	base for test data and test routine
00002AD8	00002B18			1956+T45	DC	A(X45)	address of test routine
00002ADC	002D			1957+	DC	H' 45'	test number
00002ADE	00			1958+	DC	X' 00'	
00002ADF	03			1959+	DC	HL1' 3'	m4
00002AE0	E5C1E5C7 D3404040			1960+	DC	CL8' VAVGL'	instruction name
00002AE8	00002B50			1961+	DC	A(RE45+16)	address of v2 source
00002AEC	00002B60			1962+	DC	A(RE45+32)	address of v3 source
00002AF0	00000010			1963+	DC	A(16)	result length
00002AF4	00002B40			1964+REA45	DC	A(RE45)	result address
00002AF8	00000000 00000000			1965+	DS	FD	gap
00002B00	00000000 00000000			1966+V1045	DS	XL16	V1 output
00002B08	00000000 00000000						
00002B10	00000000 00000000			1967+	DS	FD	gap
				1968+*			
00002B18				1969+X45	DS	OF	
00002B18	E310 5010 0014		00000010	1970+	LGF	R1, V2ADDR	load v2 source
00002B1E	E761 0000 0806		00000000	1971+	VL	v22, 0(R1)	use v22 to test decoder
00002B24	E310 5014 0014		00000014	1972+	LGF	R1, V3ADDR	load v3 source
00002B2A	E771 0000 0806		00000000	1973+	VL	v23, 0(R1)	use v23 to test decoder
00002B30	E766 7000 3EF0			1974+	VAVGL	V22, V22, V23, 3	test instruction (dest is a source)
00002B36	E760 5028 080E		00002B00	1975+	VST	V22, V1045	save v1 output
00002B3C	07FB			1976+	BR	R11	return
00002B40				1977+RE45	DC	OF	xl16 expected result
00002B40				1978+	DROP	R5	
00002B40	7F7F7F7F 7F7F7F7F			1979	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002B48	7F7F7F7F 7F7F7F7F						
00002B50	7C7C7C7C 7C7C7C7C			1980	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002B58	7C7C7C7C 7C7C7C7C						
00002B60	82828282 82828282			1981	DC	XL16' 82828282828282828282828282828282'	v3
00002B68	82828282 82828282						
				1982			
				1983	* Doubleword		
				1984	VRR_C	VAVGL, 3	
00002B70				1985+	DS	OFD	
00002B70		00002B70		1986+	USING	*, R5	base for test data and test routine
00002B70	00002BB0			1987+T46	DC	A(X46)	address of test routine
00002B74	002E			1988+	DC	H' 46'	test number
00002B76	00			1989+	DC	X' 00'	
00002B77	03			1990+	DC	HL1' 3'	m4
00002B78	E5C1E5C7 D3404040			1991+	DC	CL8' VAVGL'	instruction name
00002B80	00002BE8			1992+	DC	A(RE46+16)	address of v2 source
00002B84	00002BF8			1993+	DC	A(RE46+32)	address of v3 source
00002B88	00000010			1994+	DC	A(16)	result length
00002B8C	00002BD8			1995+REA46	DC	A(RE46)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002B90	00000000 00000000			1996+	DS	FD	gap
00002B98	00000000 00000000			1997+V1046	DS	XL16	V1 output
00002BA0	00000000 00000000						
00002BA8	00000000 00000000			1998+	DS	FD	gap
				1999+*			
00002BB0				2000+X46	DS	OF	
00002BB0	E310 5010 0014		00000010	2001+	LGF	R1, V2ADDR	load v2 source
00002BB6	E761 0000 0806		00000000	2002+	VL	v22, 0(R1)	use v22 to test decoder
00002BBC	E310 5014 0014		00000014	2003+	LGF	R1, V3ADDR	load v3 source
00002BC2	E771 0000 0806		00000000	2004+	VL	v23, 0(R1)	use v23 to test decoder
00002BC8	E766 7000 3EF0			2005+	VAVGL	V22, V22, V23, 3	test instruction (dest is a source)
00002BCE	E760 5028 080E		00002B98	2006+	VST	V22, V1046	save v1 output
00002BD4	07FB			2007+	BR	R11	return
00002BD8				2008+RE46	DC	OF	xl16 expected result
00002BD8				2009+	DROP	R5	
00002BD8	7FFFFFFFF FFFFFFFC			2010	DC	XL16' 7FFFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFFC'	expected result
00002BE0	7FFFFFFFF FFFFFFFC						
00002BE8	7FFFFFFFF FFFFFFFC			2011	DC	XL16' 7FFFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFFC'	v2
00002BF0	7FFFFFFFF FFFFFFFC						
00002BF8	7FFFFFFFF FFFFFFFC			2012	DC	XL16' 7FFFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFFC'	v3
00002C00	7FFFFFFFF FFFFFFFC						
				2013			
				2014 * Doubleword			
00002C08				2015	VRR_C	VAVGL, 3	
00002C08		00002C08		2016+	DS	OFD	
00002C08	00002C48			2017+	USING	*, R5	base for test data and test routine
00002C0C	002F			2018+T47	DC	A(X47)	address of test routine
00002C0E	00			2019+	DC	H' 47'	test number
00002C0F	03			2020+	DC	X' 00'	
00002C10	E5C1E5C7 D3404040			2021+	DC	HL1' 3'	m4
00002C18	00002C80			2022+	DC	CL8' VAVGL'	instruction name
00002C1C	00002C90			2023+	DC	A(RE47+16)	address of v2 source
00002C20	00000010			2024+	DC	A(RE47+32)	address of v3 source
00002C24	00002C70			2025+	DC	A(16)	result length
00002C28	00000000 00000000			2026+REA47	DC	A(RE47)	result address
00002C30	00000000 00000000			2027+	DS	FD	gap
00002C38	00000000 00000000			2028+V1047	DS	XL16	V1 output
00002C40	00000000 00000000						
				2029+	DS	FD	gap
				2030+*			
00002C48				2031+X47	DS	OF	
00002C48	E310 5010 0014		00000010	2032+	LGF	R1, V2ADDR	load v2 source
00002C4E	E761 0000 0806		00000000	2033+	VL	v22, 0(R1)	use v22 to test decoder
00002C54	E310 5014 0014		00000014	2034+	LGF	R1, V3ADDR	load v3 source
00002C5A	E771 0000 0806		00000000	2035+	VL	v23, 0(R1)	use v23 to test decoder
00002C60	E766 7000 3EF0			2036+	VAVGL	V22, V22, V23, 3	test instruction (dest is a source)
00002C66	E760 5028 080E		00002C30	2037+	VST	V22, V1047	save v1 output
00002C6C	07FB			2038+	BR	R11	return
00002C70				2039+RE47	DC	OF	xl16 expected result
00002C70				2040+	DROP	R5	
00002C70	7FFFFFFFF FFFFFFFF			2041	DC	XL16' 7FFFFFFFFFFFFFFFFF7FFFFFFFFFFFFFFFFF'	expected result
00002C78	7FFFFFFFF FFFFFFFF						
00002C80	80000000 00000002			2042	DC	XL16' 80000000000000028000000000000002'	v2
00002C88	80000000 00000002						
00002C90	7FFFFFFFF FFFFFFFC			2043	DC	XL16' 7FFFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFFC'	v3
00002C98	7FFFFFFFF FFFFFFFC						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2044		
				2045 * Doubleword		
00002CA0				2046 VRR_C VAVGL, 3		
00002CA0		00002CA0		2047+ DS OFD		
00002CA0	00002CE0			2048+ USING *, R5		base for test data and test routine
00002CA4	0030			2049+T48 DC A(X48)		address of test routine
00002CA6	00			2050+ DC H' 48'		test number
00002CA7	03			2051+ DC X' 00'		
00002CA8	E5C1E5C7 D3404040			2052+ DC HL1' 3'		m4
00002CB0	00002D18			2053+ DC CL8' VAVGL'		instruction name
00002CB4	00002D28			2054+ DC A(RE48+16)		address of v2 source
00002CB8	00000010			2055+ DC A(RE48+32)		address of v3 source
00002CBC	00002D08			2056+ DC A(16)		result length
00002CC0	00000000 00000000			2057+REA48 DC A(RE48)		result address
00002CC8	00000000 00000000			2058+ DS FD		gap
00002CD0	00000000 00000000			2059+V1048 DS XL16		V1 output
00002CD8	00000000 00000000			2060+ DS FD		gap
				2061+*		
00002CE0				2062+X48 DS OF		
00002CE0	E310 5010 0014	00000010		2063+ LGF R1, V2ADDR		load v2 source
00002CE6	E761 0000 0806	00000000		2064+ VL v22, 0(R1)		use v22 to test decoder
00002CEC	E310 5014 0014	00000014		2065+ LGF R1, V3ADDR		load v3 source
00002CF2	E771 0000 0806	00000000		2066+ VL v23, 0(R1)		use v23 to test decoder
00002CF8	E766 7000 3EF0			2067+ VAVGL V22, V22, V23, 3		test instruction (dest is a source)
00002CFE	E760 5028 080E	00002CC8		2068+ VST V22, V1048		save v1 output
00002D04	07FB			2069+ BR R11		return
00002D08				2070+RE48 DC OF		xl16 expected result
00002D08				2071+ DROP R5		
00002D08	7FFFFFFFF FFFFFFFF			2072 DC XL16' 7FFFFFFFFFFFFFFFFF7FFFFFFFFFFFFFFFFF'		expected result
00002D10	7FFFFFFFF FFFFFFFF					
00002D18	7FFFFFFFF FFFFFFFFC			2073 DC XL16' 7FFFFFFFFFFFFFFFFFC7FFFFFFFFFFFFFFFFFC'		v2
00002D20	7FFFFFFFF FFFFFFFFC					
00002D28	80000000 00000002			2074 DC XL16' 80000000000000028000000000000002'		v3
00002D30	80000000 00000002					
				2075		
				2076 * Doubleword		
				2077 VRR_C VAVGL, 3		
00002D38				2078+ DS OFD		
00002D38		00002D38		2079+ USING *, R5		base for test data and test routine
00002D38	00002D78			2080+T49 DC A(X49)		address of test routine
00002D3C	0031			2081+ DC H' 49'		test number
00002D3E	00			2082+ DC X' 00'		
00002D3F	03			2083+ DC HL1' 3'		m4
00002D40	E5C1E5C7 D3404040			2084+ DC CL8' VAVGL'		instruction name
00002D48	00002DB0			2085+ DC A(RE49+16)		address of v2 source
00002D4C	00002DC0			2086+ DC A(RE49+32)		address of v3 source
00002D50	00000010			2087+ DC A(16)		result length
00002D54	00002DA0			2088+REA49 DC A(RE49)		result address
00002D58	00000000 00000000			2089+ DS FD		gap
00002D60	00000000 00000000			2090+V1049 DS XL16		V1 output
00002D68	00000000 00000000					
00002D70	00000000 00000000			2091+ DS FD		gap
				2092+*		
00002D78				2093+X49 DS OF		
00002D78	E310 5010 0014	00000010		2094+ LGF R1, V2ADDR		load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002D7E	E761 0000 0806		00000000	2095+	VL	v22, 0(R1)	use v22 to test decoder
00002D84	E310 5014 0014		00000014	2096+	LGF	R1, V3ADDR	load v3 source
00002D8A	E771 0000 0806		00000000	2097+	VL	v23, 0(R1)	use v23 to test decoder
00002D90	E766 7000 3EF0			2098+	VAVGL	V22, V22, V23, 3	test instruction (dest is a source)
00002D96	E760 5028 080E		00002D60	2099+	VST	V22, V1049	save v1 output
00002D9C	07FB			2100+	BR	R11	return
00002DA0				2101+RE49	DC	0F	xl16 expected result
00002DA0				2102+	DROP	R5	
00002DA0	80000000 00000002			2103	DC	XL16' 80000000000000002800000000000002'	expected result
00002DA8	80000000 00000002						
00002DB0	80000000 00000002			2104	DC	XL16' 80000000000000002800000000000002'	v2
00002DB8	80000000 00000002						
00002DC0	80000000 00000002			2105	DC	XL16' 80000000000000002800000000000002'	v3
00002DC8	80000000 00000002						
				2106			
				2107			
				2108			
				2109 * Quadword			
00002DD0				2110	VRR_C	VAVGL, 4	
00002DD0		00002DD0		2111+	DS	0FD	
00002DD0	00002E10			2112+	USING	*, R5	base for test data and test routine
00002DD4	0032			2113+T50	DC	A(X50)	address of test routine
00002DD6	00			2114+	DC	H' 50'	test number
00002DD7	04			2115+	DC	X' 00'	
00002DD8	E5C1E5C7 D3404040			2116+	DC	HL1' 4'	m4
00002DE0	00002E48			2117+	DC	CL8' VAVGL'	instruction name
00002DE4	00002E58			2118+	DC	A(RE50+16)	address of v2 source
00002DE8	00000010			2119+	DC	A(RE50+32)	address of v3 source
00002DEC	00002E38			2120+	DC	A(16)	result length
00002DF0	00000000 00000000			2121+REA50	DC	A(RE50)	result address
00002DF8	00000000 00000000			2122+	DS	FD	gap
00002E00	00000000 00000000			2123+V1050	DS	XL16	V1 output
00002E08	00000000 00000000						
				2124+	DS	FD	gap
				2125+*			
00002E10				2126+X50	DS	0F	
00002E10	E310 5010 0014		00000010	2127+	LGF	R1, V2ADDR	load v2 source
00002E16	E761 0000 0806		00000000	2128+	VL	v22, 0(R1)	use v22 to test decoder
00002E1C	E310 5014 0014		00000014	2129+	LGF	R1, V3ADDR	load v3 source
00002E22	E771 0000 0806		00000000	2130+	VL	v23, 0(R1)	use v23 to test decoder
00002E28	E766 7000 4EF0			2131+	VAVGL	V22, V22, V23, 4	test instruction (dest is a source)
00002E2E	E760 5028 080E		00002DF8	2132+	VST	V22, V1050	save v1 output
00002E34	07FB			2133+	BR	R11	return
00002E38				2134+RE50	DC	0F	xl16 expected result
00002E38				2135+	DROP	R5	
00002E38	7F7F7F7F 7F7F7F7F			2136	DC	XL16' 7F7F7F7F7F7F7F7F7F7F7F7F7F7F7F'	expected result
00002E40	7F7F7F7F 7F7F7F7F						
00002E48	7C7C7C7C 7C7C7C7C			2137	DC	XL16' 7C7C7C7C7C7C7C7C7C7C7C7C7C7C7C'	v2
00002E50	7C7C7C7C 7C7C7C7C						
00002E58	82828282 82828282			2138	DC	XL16' 82828282828282828282828282828282'	v3
00002E60	82828282 82828282						
				2139			
				2140 * Quadword			
				2141	VRR_C	VAVGL, 4	
00002E68				2142+	DS	0FD	
00002E68		00002E68		2143+	USING	*, R5	base for test data and test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002E68	00002EA8			2144+T51	DC	A(X51)	address of test routine
00002E6C	0033			2145+	DC	H' 51'	test number
00002E6E	00			2146+	DC	X' 00'	
00002E6F	04			2147+	DC	HL1' 4'	m4
00002E70	E5C1E5C7 D3404040			2148+	DC	CL8' VAVGL'	instruction name
00002E78	00002EE0			2149+	DC	A(RE51+16)	address of v2 source
00002E7C	00002EF0			2150+	DC	A(RE51+32)	address of v3 source
00002E80	00000010			2151+	DC	A(16)	result length
00002E84	00002ED0			2152+REA51	DC	A(RE51)	result address
00002E88	00000000 00000000			2153+	DS	FD	gap
00002E90	00000000 00000000			2154+V1051	DS	XL16	V1 output
00002E98	00000000 00000000						
00002EA0	00000000 00000000			2155+	DS	FD	gap
				2156+*			
00002EA8				2157+X51	DS	0F	
00002EA8	E310 5010 0014		00000010	2158+	LGF	R1, V2ADDR	load v2 source
00002EAE	E761 0000 0806		00000000	2159+	VL	v22, 0(R1)	use v22 to test decoder
00002EB4	E310 5014 0014		00000014	2160+	LGF	R1, V3ADDR	load v3 source
00002EBA	E771 0000 0806		00000000	2161+	VL	v23, 0(R1)	use v23 to test decoder
00002EC0	E766 7000 4EF0			2162+	VAVGL	V22, V22, V23, 4	test instruction (dest is a source)
00002EC6	E760 5028 080E		00002E90	2163+	VST	V22, V1051	save v1 output
00002ECC	07FB			2164+	BR	R11	return
00002ED0				2165+RE51	DC	0F	xl16 expected result
00002ED0				2166+	DROP	R5	
00002ED0	7FFFFFFF FFFFFFFC			2167	DC	XL16' 7FFFFFFF7FFFFFFC7FFFFFFF7FFFFFFC'	expected result
00002ED8	7FFFFFFF FFFFFFFC						
00002EE0	7FFFFFFF FFFFFFFC			2168	DC	XL16' 7FFFFFFF7FFFFFFC7FFFFFFF7FFFFFFC'	v2
00002EE8	7FFFFFFF FFFFFFFC						
00002EF0	7FFFFFFF FFFFFFFC			2169	DC	XL16' 7FFFFFFF7FFFFFFC7FFFFFFF7FFFFFFC'	v3
00002EF8	7FFFFFFF FFFFFFFC						
				2170			
				2171 * Quadword			
				2172	VRR_C	VAVGL, 4	
00002F00				2173+	DS	0FD	
00002F00		00002F00		2174+	USING	*, R5	base for test data and test routine
00002F00	00002F40			2175+T52	DC	A(X52)	address of test routine
00002F04	0034			2176+	DC	H' 52'	test number
00002F06	00			2177+	DC	X' 00'	
00002F07	04			2178+	DC	HL1' 4'	m4
00002F08	E5C1E5C7 D3404040			2179+	DC	CL8' VAVGL'	instruction name
00002F10	00002F78			2180+	DC	A(RE52+16)	address of v2 source
00002F14	00002F88			2181+	DC	A(RE52+32)	address of v3 source
00002F18	00000010			2182+	DC	A(16)	result length
00002F1C	00002F68			2183+REA52	DC	A(RE52)	result address
00002F20	00000000 00000000			2184+	DS	FD	gap
00002F28	00000000 00000000			2185+V1052	DS	XL16	V1 output
00002F30	00000000 00000000						
00002F38	00000000 00000000			2186+	DS	FD	gap
				2187+*			
00002F40				2188+X52	DS	0F	
00002F40	E310 5010 0014		00000010	2189+	LGF	R1, V2ADDR	load v2 source
00002F46	E761 0000 0806		00000000	2190+	VL	v22, 0(R1)	use v22 to test decoder
00002F4C	E310 5014 0014		00000014	2191+	LGF	R1, V3ADDR	load v3 source
00002F52	E771 0000 0806		00000000	2192+	VL	v23, 0(R1)	use v23 to test decoder
00002F58	E766 7000 4EF0			2193+	VAVGL	V22, V22, V23, 4	test instruction (dest is a source)
00002F5E	E760 5028 080E		00002F28	2194+	VST	V22, V1052	save v1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002F64	07FB			2195+	BR	R11	return
00002F68				2196+RE52	DC	0F	xl16 expected result
00002F68				2197+	DROP	R5	
00002F68	7FFFFFFF FFFFFFFF			2198	DC	XL16' 7FFFFFFF7FFFFFFF'	expected result
00002F70	7FFFFFFF FFFFFFFF						
00002F78	80000000 00000002			2199	DC	XL16' 80000000000000028000000000000002'	v2
00002F80	80000000 00000002						
00002F88	7FFFFFFF FFFFFFFFC			2200	DC	XL16' 7FFFFFFFC7FFFFFFFC'	v3
00002F90	7FFFFFFF FFFFFFFFC						
				2201			
				2202 * Quadword			
00002F98				2203	VRR_C	VAVGL, 4	
00002F98		00002F98		2204+	DS	0FD	
00002F98	00002FD8			2205+	USING	*, R5	base for test data and test routine
00002F9C	0035			2206+T53	DC	A(X53)	address of test routine
00002F9E	00			2207+	DC	H' 53'	test number
00002F9F	04			2208+	DC	X' 00'	
00002FA0	E5C1E5C7 D3404040			2209+	DC	HL1' 4'	m4
00002FA8	00003010			2210+	DC	CL8' VAVGL'	instruction name
00002FAC	00003020			2211+	DC	A(RE53+16)	address of v2 source
00002FB0	00000010			2212+	DC	A(RE53+32)	address of v3 source
00002FB4	00003000			2213+	DC	A(16)	result length
00002FB8	00000000 00000000			2214+REA53	DC	A(RE53)	result address
00002FC0	00000000 00000000			2215+	DS	FD	gap
00002FC8	00000000 00000000			2216+V1053	DS	XL16	V1 output
00002FD0	00000000 00000000						
				2217+	DS	FD	gap
				2218+*			
00002FD8				2219+X53	DS	0F	
00002FD8	E310 5010 0014		00000010	2220+	LGF	R1, V2ADDR	load v2 source
00002FDE	E761 0000 0806		00000000	2221+	VL	v22, 0(R1)	use v22 to test decoder
00002FE4	E310 5014 0014		00000014	2222+	LGF	R1, V3ADDR	load v3 source
00002FEA	E771 0000 0806		00000000	2223+	VL	v23, 0(R1)	use v23 to test decoder
00002FF0	E766 7000 4EF0			2224+	VAVGL	V22, V22, V23, 4	test instruction (dest is a source)
00002FF6	E760 5028 080E		00002FC0	2225+	VST	V22, V1053	save v1 output
00002FFC	07FB			2226+	BR	R11	return
00003000				2227+RE53	DC	0F	xl16 expected result
00003000				2228+	DROP	R5	
00003000	7FFFFFFF FFFFFFFF			2229	DC	XL16' 7FFFFFFF7FFFFFFF'	expected result
00003008	7FFFFFFF FFFFFFFF						
00003010	7FFFFFFF FFFFFFFFC			2230	DC	XL16' 7FFFFFFFC7FFFFFFFC'	v2
00003018	7FFFFFFF FFFFFFFFC						
00003020	80000000 00000002			2231	DC	XL16' 80000000000000028000000000000002'	v3
00003028	80000000 00000002						
				2232			
				2233 * Quadword			
00003030				2234	VRR_C	VAVGL, 4	
00003030		00003030		2235+	DS	0FD	
00003030	00003070			2236+	USING	*, R5	base for test data and test routine
00003034	0036			2237+T54	DC	A(X54)	address of test routine
00003036	00			2238+	DC	H' 54'	test number
00003037	04			2239+	DC	X' 00'	
00003038	E5C1E5C7 D3404040			2240+	DC	HL1' 4'	m4
00003040	000030A8			2241+	DC	CL8' VAVGL'	instruction name
00003044	000030B8			2242+	DC	A(RE54+16)	address of v2 source
				2243+	DC	A(RE54+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003048	00000010			2244+	DC	A(16)	result length
0000304C	00003098			2245+REA54	DC	A(RE54)	result address
00003050	00000000 00000000			2246+	DS	FD	gap
00003058	00000000 00000000			2247+V1054	DS	XL16	V1 output
00003060	00000000 00000000						
00003068	00000000 00000000			2248+	DS	FD	gap
				2249+*			
00003070				2250+X54	DS	OF	
00003070	E310 5010 0014		00000010	2251+	LGF	R1, V2ADDR	load v2 source
00003076	E761 0000 0806		00000000	2252+	VL	v22, 0(R1)	use v22 to test decoder
0000307C	E310 5014 0014		00000014	2253+	LGF	R1, V3ADDR	load v3 source
00003082	E771 0000 0806		00000000	2254+	VL	v23, 0(R1)	use v23 to test decoder
00003088	E766 7000 4EF0			2255+	VAVGL	V22, V22, V23, 4	test instruction (dest is a source)
0000308E	E760 5028 080E		00003058	2256+	VST	V22, V1054	save v1 output
00003094	07FB			2257+	BR	R11	return
00003098				2258+RE54	DC	OF	xl16 expected result
00003098				2259+	DROP	R5	
00003098	80000000 00000002			2260	DC	XL16' 80000000000000002800000000000002'	expected result
000030A0	80000000 00000002						
000030A8	80000000 00000002			2261	DC	XL16' 80000000000000002800000000000002'	v2
000030B0	80000000 00000002						
000030B8	80000000 00000002			2262	DC	XL16' 80000000000000002800000000000002'	v3
000030C0	80000000 00000002						
				2263			
				2264			
				2265			
000030C8	00000000			2266	DC	F' 0'	END OF TABLE
000030CC	00000000			2267	DC	F' 0'	
				2268 *			
				2269 *	table of pointers to individual load test		
				2270 *			
000030D0				2271 E7TESTS	DS	OF	
				2272	PTTABLE		
000030D0				2273+TTABLE	DS	OF	
000030D0	000010B8			2274+	DC	A(T1)	TEST &CUR
000030D4	00001150			2275+	DC	A(T2)	TEST &CUR
000030D8	000011E8			2276+	DC	A(T3)	TEST &CUR
000030DC	00001280			2277+	DC	A(T4)	TEST &CUR
000030E0	00001318			2278+	DC	A(T5)	TEST &CUR
000030E4	000013B0			2279+	DC	A(T6)	TEST &CUR
000030E8	00001448			2280+	DC	A(T7)	TEST &CUR
000030EC	000014E0			2281+	DC	A(T8)	TEST &CUR
000030F0	00001578			2282+	DC	A(T9)	TEST &CUR
000030F4	00001610			2283+	DC	A(T10)	TEST &CUR
000030F8	000016A8			2284+	DC	A(T11)	TEST &CUR
000030FC	00001740			2285+	DC	A(T12)	TEST &CUR
00003100	000017D8			2286+	DC	A(T13)	TEST &CUR
00003104	00001870			2287+	DC	A(T14)	TEST &CUR
00003108	00001908			2288+	DC	A(T15)	TEST &CUR
0000310C	000019A0			2289+	DC	A(T16)	TEST &CUR
00003110	00001A38			2290+	DC	A(T17)	TEST &CUR
00003114	00001AD0			2291+	DC	A(T18)	TEST &CUR
00003118	00001B68			2292+	DC	A(T19)	TEST &CUR
0000311C	00001C00			2293+	DC	A(T20)	TEST &CUR
00003120	00001C98			2294+	DC	A(T21)	TEST &CUR
00003124	00001D30			2295+	DC	A(T22)	TEST &CUR

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2335 *****
				2336 * Register equates
				2337 *****
		00000000	00000001	2339 R0 EQU 0
		00000001	00000001	2340 R1 EQU 1
		00000002	00000001	2341 R2 EQU 2
		00000003	00000001	2342 R3 EQU 3
		00000004	00000001	2343 R4 EQU 4
		00000005	00000001	2344 R5 EQU 5
		00000006	00000001	2345 R6 EQU 6
		00000007	00000001	2346 R7 EQU 7
		00000008	00000001	2347 R8 EQU 8
		00000009	00000001	2348 R9 EQU 9
		0000000A	00000001	2349 R10 EQU 10
		0000000B	00000001	2350 R11 EQU 11
		0000000C	00000001	2351 R12 EQU 12
		0000000D	00000001	2352 R13 EQU 13
		0000000E	00000001	2353 R14 EQU 14
		0000000F	00000001	2354 R15 EQU 15
				2356 *****
				2357 * Register equates
				2358 *****
		00000000	00000001	2360 V0 EQU 0
		00000001	00000001	2361 V1 EQU 1
		00000002	00000001	2362 V2 EQU 2
		00000003	00000001	2363 V3 EQU 3
		00000004	00000001	2364 V4 EQU 4
		00000005	00000001	2365 V5 EQU 5
		00000006	00000001	2366 V6 EQU 6
		00000007	00000001	2367 V7 EQU 7
		00000008	00000001	2368 V8 EQU 8
		00000009	00000001	2369 V9 EQU 9
		0000000A	00000001	2370 V10 EQU 10
		0000000B	00000001	2371 V11 EQU 11
		0000000C	00000001	2372 V12 EQU 12
		0000000D	00000001	2373 V13 EQU 13
		0000000E	00000001	2374 V14 EQU 14
		0000000F	00000001	2375 V15 EQU 15
		00000010	00000001	2376 V16 EQU 16
		00000011	00000001	2377 V17 EQU 17
		00000012	00000001	2378 V18 EQU 18
		00000013	00000001	2379 V19 EQU 19
		00000014	00000001	2380 V20 EQU 20
		00000015	00000001	2381 V21 EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES														
BEGIN	I	00000200	2	162	128	158	159	160											
CTLR0	F	0000053C	4	391	172	173	174	175											
DECNUM	C	00001073	16	443	305	307	313	315											
E7TEST	4	00000000	64	457	254														
E7TESTS	F	000030D0	4	2271	247														
EDIT	X	00001047	18	438	306	314													
ENDTEST	U	000003CE	1	291	252														
EOJ	I	00000520	4	381	207	240	294												
EOJPSW	D	00000510	8	379	381														
FAILCONT	U	000003BE	1	281															
FAILED	F	00001000	4	420	283	292													
FAILMSG	U	000003BA	1	275	265														
FAILPSW	D	00000528	8	383	385														
FAILTEST	I	00000538	4	385	295														
FB0001	F	00000280	8	191	195	196	198												
FB0002	F	00000330	8	224	228	229	231												
IMAGE	1	00000000	12728	0															
K	U	00000400	1	404	405	406	407												
K64	U	00010000	1	406															
M4	U	00000007	1	461	312														
MB	U	00100000	1	407															
MSG	I	00000458	4	341	206	239	324												
MSGCMD	C	000004A6	9	371	354	355													
MSGMSG	C	000004AF	95	372	348	369	346												
MSGMVC	I	000004A0	6	369	352														
MSGOK	I	0000046E	2	350	347														
MSGRET	I	0000048E	4	365	358	361													
MSGSAVE	F	00000494	4	368	344	365													
NEXTE6	U	00000384	1	249	268	286													
OPNAME	C	00000008	8	463	310														
PAGE	U	00001000	1	405															
PRT3	C	0000105D	18	441	306	307	308	314	315	316									
PRTLNE	C	00001008	16	426	433	323													
PRTLNG	U	0000003F	1	433	322														
PRTM4	C	00001044	2	431	316														
PRTNAME	C	00001033	8	429	310														
PRTNUM	C	00001018	3	427	308														
R0	U	00000000	1	2339	122	172	175	195	197	198	199	204	228	230	231	232	237		
R1	U	00000001	1	2340	256	257	282	283	321	322	325	341	344	346	348	350	365		
					205	238	263	264	292	293	323	355	369	590	591	592	593		
					621	622	623	624	652	653	654	655	683	684	685	686	714		
					715	716	717	745	746	747	748	776	777	778	779	810	811		
					812	813	841	842	843	844	872	873	874	875	903	904	905		
					906	934	935	936	937	965	966	967	968	996	997	998	999		
					1030	1031	1032	1033	1061	1062	1063	1064	1092	1093	1094	1095	1123		
					1124	1125	1126	1155	1156	1157	1158	1186	1187	1188	1189	1217	1218		
					1219	1220	1251	1252	1253	1254	1282	1283	1284	1285	1313	1314	1315		
					1316	1344	1345	1346	1347	1375	1376	1377	1378	1406	1407	1408	1409		
					1437	1438	1439	1440	1471	1472	1473	1474	1502	1503	1504	1505	1533		
					1534	1535	1536	1564	1565	1566	1567	1595	1596	1597	1598	1626	1627		
					1628	1629	1657	1658	1659	1660	1688	1689	1690	1691	1719	1720	1721		
					1722	1750	1751	1752	1753	1781	1782	1783	1784	1812	1813	1814	1815		
					1843	1844	1845	1846	1877	1878	1879	1880	1908	1909	1910	1911	1939		
					1940	1941	1942	1970	1971	1972	1973	2001	2002	2003	2004	2032	2033		
					2034	2035	2063	2064	2065	2066	2094	2095	2096	2097	2127	2128	2129		
					2130	2158	2159	2160	2161	2189	2190	2191	2192	2220	2221	2222	2223		

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
					2251	2252	2253	2254										
R10	U	0000000A	1	2349	160	169	170											
R11	U	0000000B	1	2350	260	261	596	627	658	689	720	751	782	816	847	878	909	
					940	971	1002	1036	1067	1098	1129	1161	1192	1223	1257	1288	1319	
					1350	1381	1412	1443	1477	1508	1539	1570	1601	1632	1663	1694	1725	
					1756	1787	1818	1849	1883	1914	1945	1976	2007	2038	2069	2100	2133	
					2164	2195	2226	2257										
R12	U	0000000C	1	2351	247	250	267	285										
R13	U	0000000D	1	2352														
R14	U	0000000E	1	2353														
R15	U	0000000F	1	2354	276	301	328	329										
R2	U	00000002	1	2341	206	239	304	305	312	313	321	324	325	342	344	350	351	
					352	354	360	365	366									
R3	U	00000003	1	2342														
R4	U	00000004	1	2343														
R5	U	00000005	1	2344	250	251	254	302	327	575	598	606	629	637	660	668	691	
					699	722	730	753	761	784	795	818	826	849	857	880	888	
					911	919	942	950	973	981	1004	1015	1038	1046	1069	1077	1100	
					1108	1131	1140	1163	1171	1194	1202	1225	1236	1259	1267	1290	1298	
					1321	1329	1352	1360	1383	1391	1414	1422	1445	1456	1479	1487	1510	
					1518	1541	1549	1572	1580	1603	1611	1634	1642	1665	1673	1696	1704	
					1727	1735	1758	1766	1789	1797	1820	1828	1851	1862	1885	1893	1916	
					1924	1947	1955	1978	1986	2009	2017	2040	2048	2071	2079	2102	2112	
					2135	2143	2166	2174	2197	2205	2228	2236	2259					
R6	U	00000006	1	2345														
R7	U	00000007	1	2346														
R8	U	00000008	1	2347	158	162	163	164	166									
R9	U	00000009	1	2348	159	166	167	169										
RE1	F	00001120	4	597	581	582	584											
RE10	F	00001678	4	879	863	864	866											
RE11	F	00001710	4	910	894	895	897											
RE12	F	000017A8	4	941	925	926	928											
RE13	F	00001840	4	972	956	957	959											
RE14	F	000018D8	4	1003	987	988	990											
RE15	F	00001970	4	1037	1021	1022	1024											
RE16	F	00001A08	4	1068	1052	1053	1055											
RE17	F	00001AA0	4	1099	1083	1084	1086											
RE18	F	00001B38	4	1130	1114	1115	1117											
RE19	F	00001BD0	4	1162	1146	1147	1149											
RE2	F	000011B8	4	628	612	613	615											
RE20	F	00001C68	4	1193	1177	1178	1180											
RE21	F	00001D00	4	1224	1208	1209	1211											
RE22	F	00001D98	4	1258	1242	1243	1245											
RE23	F	00001E30	4	1289	1273	1274	1276											
RE24	F	00001EC8	4	1320	1304	1305	1307											
RE25	F	00001F60	4	1351	1335	1336	1338											
RE26	F	00001FF8	4	1382	1366	1367	1369											
RE27	F	00002090	4	1413	1397	1398	1400											
RE28	F	00002128	4	1444	1428	1429	1431											
RE29	F	000021C0	4	1478	1462	1463	1465											
RE3	F	00001250	4	659	643	644	646											
RE30	F	00002258	4	1509	1493	1494	1496											
RE31	F	000022F0	4	1540	1524	1525	1527											
RE32	F	00002388	4	1571	1555	1556	1558											
RE33	F	00002420	4	1602	1586	1587	1589											
RE34	F	000024B8	4	1633	1617	1618	1620											

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES			
RE35	F	00002550	4	1664	1648	1649	1651	
RE36	F	000025E8	4	1695	1679	1680	1682	
RE37	F	00002680	4	1726	1710	1711	1713	
RE38	F	00002718	4	1757	1741	1742	1744	
RE39	F	000027B0	4	1788	1772	1773	1775	
RE4	F	000012E8	4	690	674	675	677	
RE40	F	00002848	4	1819	1803	1804	1806	
RE41	F	000028E0	4	1850	1834	1835	1837	
RE42	F	00002978	4	1884	1868	1869	1871	
RE43	F	00002A10	4	1915	1899	1900	1902	
RE44	F	00002AA8	4	1946	1930	1931	1933	
RE45	F	00002B40	4	1977	1961	1962	1964	
RE46	F	00002BD8	4	2008	1992	1993	1995	
RE47	F	00002C70	4	2039	2023	2024	2026	
RE48	F	00002D08	4	2070	2054	2055	2057	
RE49	F	00002DA0	4	2101	2085	2086	2088	
RE5	F	00001380	4	721	705	706	708	
RE50	F	00002E38	4	2134	2118	2119	2121	
RE51	F	00002ED0	4	2165	2149	2150	2152	
RE52	F	00002F68	4	2196	2180	2181	2183	
RE53	F	00003000	4	2227	2211	2212	2214	
RE54	F	00003098	4	2258	2242	2243	2245	
RE6	F	00001418	4	752	736	737	739	
RE7	F	000014B0	4	783	767	768	770	
RE8	F	00001548	4	817	801	802	804	
RE9	F	000015E0	4	848	832	833	835	
REA1	A	000010D4	4	584				
REA10	A	0000162C	4	866				
REA11	A	000016C4	4	897				
REA12	A	0000175C	4	928				
REA13	A	000017F4	4	959				
REA14	A	0000188C	4	990				
REA15	A	00001924	4	1024				
REA16	A	000019BC	4	1055				
REA17	A	00001A54	4	1086				
REA18	A	00001AEC	4	1117				
REA19	A	00001B84	4	1149				
REA2	A	0000116C	4	615				
REA20	A	00001C1C	4	1180				
REA21	A	00001CB4	4	1211				
REA22	A	00001D4C	4	1245				
REA23	A	00001DE4	4	1276				
REA24	A	00001E7C	4	1307				
REA25	A	00001F14	4	1338				
REA26	A	00001FAC	4	1369				
REA27	A	00002044	4	1400				
REA28	A	000020DC	4	1431				
REA29	A	00002174	4	1465				
REA3	A	00001204	4	646				
REA30	A	0000220C	4	1496				
REA31	A	000022A4	4	1527				
REA32	A	0000233C	4	1558				
REA33	A	000023D4	4	1589				
REA34	A	0000246C	4	1620				
REA35	A	00002504	4	1651				
REA36	A	0000259C	4	1682				

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA37	A	00002634	4	1713		
REA38	A	000026CC	4	1744		
REA39	A	00002764	4	1775		
REA4	A	0000129C	4	677		
REA40	A	000027FC	4	1806		
REA41	A	00002894	4	1837		
REA42	A	0000292C	4	1871		
REA43	A	000029C4	4	1902		
REA44	A	00002A5C	4	1933		
REA45	A	00002AF4	4	1964		
REA46	A	00002B8C	4	1995		
REA47	A	00002C24	4	2026		
REA48	A	00002CBC	4	2057		
REA49	A	00002D54	4	2088		
REA5	A	00001334	4	708		
REA50	A	00002DEC	4	2121		
REA51	A	00002E84	4	2152		
REA52	A	00002F1C	4	2183		
REA53	A	00002FB4	4	2214		
REA54	A	0000304C	4	2245		
REA6	A	000013CC	4	739		
REA7	A	00001464	4	770		
REA8	A	000014FC	4	804		
REA9	A	00001594	4	835		
READDR	A	0000001C	4	467	263	
REG2LOW	U	000000DD	1	410		
REG2PATT	U	AABBCCDD	1	409		
RELEN	A	00000018	4	466		
RPTDWSAV	D	00000448	8	334	321	325
RPTERROR	I	000003DC	4	301	276	
RPTSAVE	F	00000440	4	331	301	328
RPTSVR5	F	00000444	4	332	302	327
SKL0001	U	0000004E	1	188	204	
SKL0002	U	0000004E	1	221	237	
SKT0001	C	0000022A	20	185	188	205
SKT0002	C	000002D4	20	218	221	238
SVOLDPSW	U	00000140	0	124		
T1	A	000010B8	4	576	2274	
T10	A	00001610	4	858	2283	
T11	A	000016A8	4	889	2284	
T12	A	00001740	4	920	2285	
T13	A	000017D8	4	951	2286	
T14	A	00001870	4	982	2287	
T15	A	00001908	4	1016	2288	
T16	A	000019A0	4	1047	2289	
T17	A	00001A38	4	1078	2290	
T18	A	00001AD0	4	1109	2291	
T19	A	00001B68	4	1141	2292	
T2	A	00001150	4	607	2275	
T20	A	00001C00	4	1172	2293	
T21	A	00001C98	4	1203	2294	
T22	A	00001D30	4	1237	2295	
T23	A	00001DC8	4	1268	2296	
T24	A	00001E60	4	1299	2297	
T25	A	00001EF8	4	1330	2298	
T26	A	00001F90	4	1361	2299	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T27	A	00002028	4	1392	2300
T28	A	000020C0	4	1423	2301
T29	A	00002158	4	1457	2302
T3	A	000011E8	4	638	2276
T30	A	000021F0	4	1488	2303
T31	A	00002288	4	1519	2304
T32	A	00002320	4	1550	2305
T33	A	000023B8	4	1581	2306
T34	A	00002450	4	1612	2307
T35	A	000024E8	4	1643	2308
T36	A	00002580	4	1674	2309
T37	A	00002618	4	1705	2310
T38	A	000026B0	4	1736	2311
T39	A	00002748	4	1767	2312
T4	A	00001280	4	669	2277
T40	A	000027E0	4	1798	2313
T41	A	00002878	4	1829	2314
T42	A	00002910	4	1863	2315
T43	A	000029A8	4	1894	2316
T44	A	00002A40	4	1925	2317
T45	A	00002AD8	4	1956	2318
T46	A	00002B70	4	1987	2319
T47	A	00002C08	4	2018	2320
T48	A	00002CA0	4	2049	2321
T49	A	00002D38	4	2080	2322
T5	A	00001318	4	700	2278
T50	A	00002DD0	4	2113	2323
T51	A	00002E68	4	2144	2324
T52	A	00002F00	4	2175	2325
T53	A	00002F98	4	2206	2326
T54	A	00003030	4	2237	2327
T6	A	000013B0	4	731	2279
T7	A	00001448	4	762	2280
T8	A	000014E0	4	796	2281
T9	A	00001578	4	827	2282
TESTING	F	00001004	4	421	257
TNUM	H	00000004	2	459	256 304
TSUB	A	00000000	4	458	260
TTABLE	F	000030D0	4	2273	
V0	U	00000000	1	2360	
V1	U	00000001	1	2361	259
V10	U	0000000A	1	2370	
V11	U	0000000B	1	2371	
V12	U	0000000C	1	2372	
V13	U	0000000D	1	2373	
V14	U	0000000E	1	2374	
V15	U	0000000F	1	2375	
V16	U	00000010	1	2376	
V17	U	00000011	1	2377	
V18	U	00000012	1	2378	
V19	U	00000013	1	2379	
V1FUDGE	X	00001094	16	450	259
V101	X	000010E0	16	586	595
V1010	X	00001638	16	868	877
V1011	X	000016D0	16	899	908
V1012	X	00001768	16	930	939

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
V1013	X	00001800	16	961	970													
V1014	X	00001898	16	992	1001													
V1015	X	00001930	16	1026	1035													
V1016	X	000019C8	16	1057	1066													
V1017	X	00001A60	16	1088	1097													
V1018	X	00001AF8	16	1119	1128													
V1019	X	00001B90	16	1151	1160													
V102	X	00001178	16	617	626													
V1020	X	00001C28	16	1182	1191													
V1021	X	00001CC0	16	1213	1222													
V1022	X	00001D58	16	1247	1256													
V1023	X	00001DF0	16	1278	1287													
V1024	X	00001E88	16	1309	1318													
V1025	X	00001F20	16	1340	1349													
V1026	X	00001FB8	16	1371	1380													
V1027	X	00002050	16	1402	1411													
V1028	X	000020E8	16	1433	1442													
V1029	X	00002180	16	1467	1476													
V103	X	00001210	16	648	657													
V1030	X	00002218	16	1498	1507													
V1031	X	000022B0	16	1529	1538													
V1032	X	00002348	16	1560	1569													
V1033	X	000023E0	16	1591	1600													
V1034	X	00002478	16	1622	1631													
V1035	X	00002510	16	1653	1662													
V1036	X	000025A8	16	1684	1693													
V1037	X	00002640	16	1715	1724													
V1038	X	000026D8	16	1746	1755													
V1039	X	00002770	16	1777	1786													
V104	X	000012A8	16	679	688													
V1040	X	00002808	16	1808	1817													
V1041	X	000028A0	16	1839	1848													
V1042	X	00002938	16	1873	1882													
V1043	X	000029D0	16	1904	1913													
V1044	X	00002A68	16	1935	1944													
V1045	X	00002B00	16	1966	1975													
V1046	X	00002B98	16	1997	2006													
V1047	X	00002C30	16	2028	2037													
V1048	X	00002CC8	16	2059	2068													
V1049	X	00002D60	16	2090	2099													
V105	X	00001340	16	710	719													
V1050	X	00002DF8	16	2123	2132													
V1051	X	00002E90	16	2154	2163													
V1052	X	00002F28	16	2185	2194													
V1053	X	00002FC0	16	2216	2225													
V1054	X	00003058	16	2247	2256													
V106	X	000013D8	16	741	750													
V107	X	00001470	16	772	781													
V108	X	00001508	16	806	815													
V109	X	000015A0	16	837	846													
V10OUTPUT	X	00000028	16	469	264													
V2	U	00000002	1	2362														
V20	U	00000014	1	2380														
V21	U	00000015	1	2381														
V22	U	00000016	1	2382	591	594	595	622	625	626	653	656	657	684	687	688	715	
					718	719	746	749	750	777	780	781	811	814	815	842	845	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES						
X18	F	00001B10	4	1122	1109						
X19	F	00001BA8	4	1154	1141						
X2	F	00001190	4	620	607						
X20	F	00001C40	4	1185	1172						
X21	F	00001CD8	4	1216	1203						
X22	F	00001D70	4	1250	1237						
X23	F	00001E08	4	1281	1268						
X24	F	00001EA0	4	1312	1299						
X25	F	00001F38	4	1343	1330						
X26	F	00001FD0	4	1374	1361						
X27	F	00002068	4	1405	1392						
X28	F	00002100	4	1436	1423						
X29	F	00002198	4	1470	1457						
X3	F	00001228	4	651	638						
X30	F	00002230	4	1501	1488						
X31	F	000022C8	4	1532	1519						
X32	F	00002360	4	1563	1550						
X33	F	000023F8	4	1594	1581						
X34	F	00002490	4	1625	1612						
X35	F	00002528	4	1656	1643						
X36	F	000025C0	4	1687	1674						
X37	F	00002658	4	1718	1705						
X38	F	000026F0	4	1749	1736						
X39	F	00002788	4	1780	1767						
X4	F	000012C0	4	682	669						
X40	F	00002820	4	1811	1798						
X41	F	000028B8	4	1842	1829						
X42	F	00002950	4	1876	1863						
X43	F	000029E8	4	1907	1894						
X44	F	00002A80	4	1938	1925						
X45	F	00002B18	4	1969	1956						
X46	F	00002BB0	4	2000	1987						
X47	F	00002C48	4	2031	2018						
X48	F	00002CE0	4	2062	2049						
X49	F	00002D78	4	2093	2080						
X5	F	00001358	4	713	700						
X50	F	00002E10	4	2126	2113						
X51	F	00002EA8	4	2157	2144						
X52	F	00002F40	4	2188	2175						
X53	F	00002FD8	4	2219	2206						
X54	F	00003070	4	2250	2237						
X6	F	000013F0	4	744	731						
X7	F	00001488	4	775	762						
X8	F	00001520	4	809	796						
X9	F	000015B8	4	840	827						
XC0001	U	000002D0	1	208	200						
XC0002	U	00000380	1	241	233						
ZVE7TST	J	00000000	12728	121	124	126	130	134	419	122	
=A(E7TESTS)	A	0000054C	4	397	247						
=AL2(L' MSGMSG)	R	00000556	2	400	346						
=F' 1'	F	00000550	4	398	282						
=F' 2'	F	00000548	4	396	232						
=F' 64'	F	00000544	4	395	199						
=H' 0'	H	00000554	2	399	341						

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	12728	0000- 31B7	0000- 31B7
Regi on		12728	0000- 31B7	0000- 31B7
CSECT	ZVE7TST	12728	0000- 31B7	0000- 31B7

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-01-MinMaxAvg.asm
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**** NO ERRORS FOUND ****